Design of Low-Voltage Analog Amplifiers Using Floating-Gate Transistors

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Chapter 1

Introduction

The main subject of this thesis, is characterization of low-voltage/low-power amplifier design using Floating-Gate UV MOS Transistors (FGUVMOS). The objective of low-voltage/low-power electronic research, is to develop methods and circuits for systems operating at low-voltage power-supply [19].

Why do we need low-voltage Amplifiers? One reason is because of the continuing down-scaling of processes, the channel length is scaled down to sub-microns, and the thickness of the gate oxide is just nanometers. Then we need to reduce the power supply to ensure device reliability. Another reason is the use of portable equipment, sensors and portable medical monitoring instruments, in order to have an acceptable operating time from the batteries, and we have to lower the supply voltage, to reduce the power consumption.

Reducing the Supply Voltage

The minimum supply voltage in traditional low-voltage circuits may be defined as:

\[ V_{sup,min} = 2(V_{gs} + V_{sat}) \]

The low-voltage circuits are able to operate on a supply voltage, \( V_{dd} \) of two stacked gate-source voltages and two saturation voltages [11]. Low-voltage circuit are circuits which operate with power supply \( V_{dd} \) less than 3V. There are amplifiers available today, using 1 Volt single supply voltage [24]. If we look at the power consumption in a digital CMOS circuit, the good news is that it follows a square law, hence great power savings are realized just for a small reduction in the power supply. However, when looking at a digital design with a power supply of 3.0V, and then reduce the supply voltage to 1.0V, the reduction in the dynamic power consumption \( \frac{P_1}{P_2} = \frac{1^2}{3^2} = 11\% \) of the original, which is a power saving of 89 %. And then when reducing the power supply from 3.0V to 0.5V the reduction is 97.3 %.

The demand for low-voltage low-power will reduce the dynamic range of an amplifier, in order to maximize the dynamic range. A low-voltage amplifier have to deal with a
voltage swing that extend from rail-to-rail \(^1\) both on the output and the input stage. When going down with the supply voltage to less than 0.5V, it is important that the output signal has an amplitude swing close to \(V_{dd}\). This means that we are getting a proper dynamic range, and a satisfying Noise Margin. Other factors which are appearing when we do reduce the power supply, is decreased signal-to-noise ratio (S/N), and reduced bandwidth.

1.1 The Floating Gate UV MOS Transistors

This thesis will deal with the design of amplifiers which uses Floating-Gate UV MOS Transistors (FGUVMOS). Floating-Gate MOS transistors have been used for several years as long term non-volatile memories [22]. By using FGUVMOS transistors the effective threshold voltage of the transistors may be tuned with UV-light [26] [4] [3] [5] [7], which is described in section 2.3. The Floating-Gate transistor may be used to design both analog and digital low-voltage/low-power circuits \((V_{dd} < 1\text{V})\). [27].

The idea of using a Floating-Gate MOS transistor is to separate the gate of a transistor from the rest of the circuit, and then inject charge on the floating gate node. In order to separate the node or the floating gate from the input, we have to use a coupling capacitor. There may be multiple inputs to each device, with a separate coupling capacitor, since the input signal is not directly coupled to the gate of the transistor.

1.2 Low-voltage/low-power Amplifier Design Using FGUVMOS transistors

The main objective of this thesis is to characterize the Floating-Gate UV MOS OTA\(^2\) circuits. A short description of the different building blocks which are used in the amplifier circuits, will be analyzed with measured and simulated results. The main focus will be DC-characteristics of the different circuits.

Floating Gate UV-MOS (FGUVMOS) transistor design, uses supply voltages less than 1 V. This is why we call them ultra low-voltage circuits. The FGUVMOS-amplifier is a rail-to-rail amplifier, the response of the FGUVMOS circuit has a signal amplitude close to \(V_{dd}\) both on the output- and on the input stage.

1.3 Presentation of the results

The measured results of the circuits will be presented, but due to limited time, not all of the circuits which are implemented have the measured results available. In that

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\(^1\) Amplifiers capable of reaching both supply “rails” are called rail-to-rail amplifiers

\(^2\) Operational Transconductance Amplifier
case the simulated results will be presented. The layout of the fabricated chip and the simulation are done with the application program Cadence ver. 4.42, which uses SpectreS as a simulation tool. The measurement equipments and methods used, is explained i appendix ??.

1.4 Overview of the Thesis

Chapter 1 gives a short introduction to the thesis, and background information.

In Chapter 2 we present the fundamental theory in the FGUV MOS transistor technology, and problems according to the UV programming process.

In Chapter 3 the common building blocks used in OTA design using FGUV MOS transistors are presented.

In Chapter 4 we do present some simple OTA’s, and analyses and characterize the results of the different amplifier circuits.

In Chapter 5 a summary and the conclusion of the thesis is provided.
CHAPTER 1. INTRODUCTION
Chapter 2

The Floating-Gate UVMOS Technology

2.1 Introduction

Floating-Gate MOS transistors have been used for several years to store digital information in EPROMS, EEPROMS and flash memories [22]. However, in 1992 a method for using multiple inputs to a floating gate [25] was discovered. The floating gate voltage was established as a weighted capacitive voltage summation. This new way of using the floating gate introduced some interesting analog and digital information-processing circuits, such as D/A converters [25] and multiple-input floating gate amplifiers [28]. Shibata and Ohmi named these devices neuMOS transistors. Yang, Andreou and Boahen named it Multiple-Input Floating-Gate Transistors, FGMOS [28]. The above mentioned methods have used Fowler-Nordheim tunneling to inject charge on the floating gate [21]. We are using UV-light to get the same result. We named our devices Floating-Gate UV MOS Transistors, FGUV MOS [26][3]. These transistors can be implemented in any commercial double-poly CMOS process.

The circuits presented in this thesis have been made by using the 0.6 μm CMOS process from AMS [1]. In such a process we let the gate (poly1) be a floating node, and we use poly2 to make the capacitor(CPOLY). When using the AMS0.6μm process, poly1 have to be larger than poly2, and by changing the area of overlap between poly1 and poly2, we are able to make several different capacitors. An example of a Cpoly capacitor is shown in figure 2.1 (b). The UV-window is made in the junction between gate and source. To make the UV-hole, we are using metall 1 and metall 2, and to make sure there is a hole in the pacification layer, we need a PAD opening over the transistor. The UV-window is seen as a box and as a circle in the source end of the transistor in figure 2.1.
2.2 FGUVMOS Transistor Model

To understand the operation of the FGUVMOS transistor, we have to discuss the capacitive division with the floating gate as the dividing node.

**Capacitive voltage divider**

When looking at figure 2.2 we can see a simple capacitive voltage division. If we are going to solve the capacitor network, we have to define \( Q = CV \). Assuming there is no charge on the middle node \( V \), we get:

\[
-Q_1 - Q_2 = -C_1(V_1 - V) - C_2(V_2 - V) = 0
\]

This gives us:

\[
V = \frac{C_1}{C_1 - C_2}V_1 + \frac{C_2}{C_1 + C_2}V_2
\]

**FGUVMOS Transistor Model in Weak Inversion**

When focusing at the multiple input n-channel FGUVMOS transistor in figure 2.1, each input has an effective coupling capacitance \( C'_i \), to the floating gate [26]. The input
signal is attenuated with a factor $K_i = \frac{C_i}{C_T}$, where $C_T$ is the total load capacitance seen from the gate. $K_i$ is called the capacitive division factor for input $i$.

We will express the behavior of a FGUVMOS circuit in equilibrium condition. This means that we are in the equilibrium point, and all control inputs are equal to $V_{dd}/2$ and the transistor current is equal to $I_{bec}$. Assuming we are using the transistors in weak inversion\(^1\), the accumulated drain current modulation of m-inputs is expressed as the product $\prod_{i=1}^{m} \exp\{\frac{1}{nU_t}(V_i - V_{dd}/2)k_i\}$. The effective drain current of a n-FGUVMOS transistor is then given by [29]:

$$I_{ds,n-MOS} = I_{bec} \prod_{i=1}^{m} \exp\{\frac{1}{nU_t}(V_i - V_{dd}/2)k_i\}$$  \hspace{1cm} (2.3)

Similar, we get the drain current of a p-FGUVMOS transistor:

$$I_{ds,p-MOS} = I_{bec} \prod_{i=1}^{m} \exp\{\frac{1}{nU_t}(V_{dd}/2 - V_i)k_i\}$$  \hspace{1cm} (2.4)

We express the min and max currents in terms of the balanced equilibrium current.

$$I_{ds}^{\text{max}} = I_{bec} \Re \Sigma_{i=1}^{m} k_i = (I_{bec})^2 / f_{ds}^{\text{max}}$$  \hspace{1cm} (2.5)

$$I_{ds}^{\text{min}} = I_{bec} \Re \Sigma_{i=1}^{m} (-k_i) = (I_{bec})^2 / f_{ds}^{\text{min}} \equiv (f_{ds}^{\text{max}})^*$$  \hspace{1cm} (2.6)

Where $\Re = \exp\{\frac{1}{2nU_t}V_{dd}\}$.

The Dynamic Range (DR) is expressed by:

$$DR = \frac{I_{ds}^{\text{max}}}{I_{ds}^{\text{min}}}$$  \hspace{1cm} (2.7)

Assuming $\Sigma_{i=1}^{m} k_i = 1$, it will then give us the the Dynamic Range equal to $\Re^2$ [3].

\(^1\)Similar analyses may be done for strong inversion as well.
FGUVMOS Design

In a FGUVMOS design there is always one p-MOS stacked on top of one n-MOS transistor. The height is always two, but it is possible to connect transistors in parallel, and each floating gate may have several inputs connected through floating capacitors shown in figure 2.1 (a). In this way we are able to compensate for the limited stacking. Even when having these limitations, it is possible to design several different FGUVMOS circuits, as showed later in the thesis.

2.3 Tuning of The FGUVMOS Transistor

In order to use the circuits in low voltage operation, we have to inject charge to the floating gate, hence we are changing the effective threshold voltage \( V_{th} \) of the transistor seen from an input. The traditional way to access or charge the floating gate is by using electron tunneling, also called Fowler/Nordheim tunneling or electron injection alternatively known as avalanche injection [21].

In order to initiate the FGUVMOS circuits, we need to access the floating gate through a resistive coupling [6]. In our case we have used UV-light (250nm) in order to charge the floating gate. When exposing the gate/source region\(^2\) to UV-light a UV-activated conductance is temporarily connecting the source/drain to the floating gate. The entire chip is exposed to UV-light, and the UV-activated conductance will disappear once the UV-light is removed. The FGUVMOS programming technique is described in a number of steps:

1. Decide the operative supply voltage \( V_{dd} \) (normal biasing).
The ideal supply voltage may be different for different applications.

2. Apply \( \frac{V_{dd}}{2} \) to all external inputs.
   When the programming is finished, all internal nodes and the output are set to \( \frac{V_{dd}}{2} \).

3. Apply the programming voltages at the supply rails \( V_- \) at \( V_{dd} \), and \( V_+ \) at \( V_{ss} \).
The supply rails are used to provide the programming voltages. The effective threshold voltage seen from the control gate, is determined by the programming voltages.

4. Terminate the programming by turning the UV-light source off when the output converges to \( \frac{V_{dd}}{2} \).

5. Set the biasing voltages to normal values.
   Use the transistor in operative mode.

\(^2\)The source and drain are switched during programming of the chip.
When we are using the transistor in *operative mode* there is no resistive connections to the floating gate, figure 2.3 (a). In the *programming mode*, the desired UV-activated conductance $G_{ngd}$ and $G_{pgd}$ appear, figure 2.3 (b). The parasitic UV-activated conductances $G_{ngs}$, $G_{nf}$, $G_{nfb}$, $G_{pgs}$, $G_{pf}$ and $G_{pgb}$, are determined by the layout and have to be considered when designing the circuit [6]. When using traditional transistors as seen in figure 2.1, the programming conductance compared to the parasitic conductance is approximately 30%. The parasitic can be reduced by narrowing the UV-window or using U-shaped transistors or ring transistors as shown in figure 2.4.

**Charge Loss**

Storing charge on a floating gate have been utilized for several years in digital design, but finding a way to control this stored charge with sufficient precision is what happens when using UV-light to program the circuit. And recently this kind of device has attracted a considerable interest as a non-volatile analog storage device and as a precision analog trimming element [22]. Experiential results show that voltage on the floating gate can be adjusted in increments of sub millivolts, and the charge loss over a period of 10 years is approximately 2% at room temperature. [22]

We have done some measurements over several months in AMS 0.8μ process, without
any noticeable problems with charge loss. We have not done any of these tests in the AMS $0.6\mu$ process. However, during the test period over three months there have not been any signs of charge loss on the floating gates.

### 2.4 Programming of the FGUVMOS Circuits

In order to use a circuit with a power supply less than 1 Volt, we have to program the effective threshold voltage $V_{th}$, and to decide the current levels also called the equilibrium current of the circuits. This section will cover some simple structures like inverters and analog inverters, and characterization of difference in programming voltages and equilibrium currents. The functionality of these circuits will be explained later in chapter 3.

#### 2.4.1 Inverter

One of the most common building block in FGUVMOS circuits is the digital inverter, seen in figure 2.5. This section will mainly focus on the programming of the circuit. As seeing in figure 2.5 this is a symmetrical design, hence it is the same amount of n-MOS and p-MOS transistors, and the same load on the floating gate on the n-MOS
and p-MOS transistor $C_{iN} = C_{iP} = C_i$. The inverter is implemented with $C_i = 18.4 fF$, and with U-shaped transistors $l = 0.6 \mu m, w = 10 \mu m$. The measured n-MOS currents $I_n$ of an inverter with $V_{dd} = 0.5 V$ are shown in figure 2.6. Typical reprogramming-time of this kind of circuit, that is the time required to change the equilibrium currents, is less than 10 minutes.

A useful operation mode is to use the circuit in weak through moderate inversion, which means we can use the circuit with an equilibrium current $I_{bec}$ ranging from $1 nA$ to $1 \mu A$\(^3\). This shows that the drain current $I_{ds}$ is exponential, as explained in the previous section. If we use a supply voltage of 0.8 V, we have to set the programming voltage $V_+$ in a range from 1.5 V to 2.2 V, and the corresponding programming voltage applied at $V_{dd}$ are shown in figure 2.8. The same current level with supply voltage equal to 0.5 V, is achieved using programming voltages $V_+$ ranging from 1.6 to 2.3 V. Finally if we are using a power supply with of 0.3 V, the programming voltage $V_+$ is 1.6 to 2.4 V.

An example; assuming we want $I_{bec} = 10 nA$ and we want to use a supply voltage of $V_{dd} = 0.5 V$. If looking at figure 2.7 and 2.8 this gives us $V_+ = 2.1 V$ and $V_- = -0.2 V$. By using these figures it is easy to find the corresponding programming voltage for the different equilibrium currents $I_{bec}$.

\(^3\)These circuits can also be used with a larger equilibrium currents, but this is just an example to illustrate the different in the programming of the circuit.
CHAPTER 2. THE FLOATING-GATE UVMOS TECHNOLOGY

Figure 2.6: Measured n-MOS current $I_n$ of an inverter with $V_{dd} = 0.5V$

Figure 2.7: Measured equilibrium current of the inverter
Figure 2.8: *Measured programming voltage of the inverter*

A twelve row inverter structure is implemented with the same transistors and the same input capacitors $C_i$. As we can see from the measured result from inverter #3, #9, #12 in figure 2.9, there is no problem to program the chip. Inverter #3 is used as a reference programming point. If focusing at figure 2.10, the switching point is exposed more detailed. The offset between inverter #3 and inverter #9 is approximately 0.5 mV, and between the switching point of #3, #12 and #9, #12 is less than 10mV. This is better than a standard inverter chain in an ordinary CMOS process.

Figure 2.11 expresses the operation range of an inverter, as we do see, if the equilibrium current $I_{sec}$ is more than 70μA, the gain is less than -1, and this is not useful to use in a chain of inverters. This is due to the transistors operating in strong inversion, hence the drain current $I_{ds}$ is linear. An inverter structure will function in strong inversion, as long as the gain is more than -1. If not, there will not be any amplification.
CHAPTER 2. THE FLOATING-GATE UVMOS TECHNOLOGY

Figure 2.9: Measured output from the inverter structure

Figure 2.10: Measured output from the inverter structure in detail
2.4. PROGRAMMING OF THE FGUVMOs CIRCUITS

2.4.2 Analog Inverters

In figure 2.12 an analog inverter is shown. An analog inverter [16] is a circuit which do have the following characteristics $V_{out} = V_{dd} - V_{in} \equiv V_{in}^*$, hence the output voltage is “analog” inverted\(^4\) of the input signal. The measured output voltage $V_{out}$ is shown in figure 2.13.

The analog inverter is almost similar to the digital inverter, but it has a diode coupled output stage. The functionality of this circuit is explained in chapter 3.2.2. The analog inverter is also a symmetrical circuit, but it has more load on the input, and a feedback from the output to the input. The circuit is implemented with input capacitor $C_i = 18.4fF$ and feedback capacitor $C_r = 14.2fF$. The transistors are U-shaped with $l = 0.6\mu m$ and $w = 10\mu m$. The measured n-MOS currents ($I_n$) are shown in figure 2.14, and typical programming time of this circuit is also approximately 10 minutes.

An acceptable operation mode is an equilibrium current $I_{bec}$ from $1nA$ to $1\mu A$, hence weak to moderate inversion. When the supply voltage is $0.8V$, a programming voltage $V_+$ from 2.2V to 3.2V is used. The respectively programming voltage of the supply rail $V_-$ is shown in figure 2.15.

When using $V_{dd} = 0.5V$ the programming voltage of $V_+$ is between 2.3V and 3.4V, and with supply of 0.3 V, the supply rail $V_+$ is in the range of 2.3V to 3.4V.

\(^4\)In other words the gain of the circuit is -1.
CHAPTER 2. THE FLOATING-GATE UVMOS TECHNOLOGY

Figure 2.12: The analog inverter

Figure 2.13: Measured output voltage of the analog inverter
2.4. PROGRAMMING OF THE FGUVMOS CIRCUITS

As the figures shows, we can use the same programming voltage $V_+$, when using the circuit with supply voltage either $0.3V$ or $0.5V$, however, there is not any significant difference of $V_{dd} = 0.8V$. This means, if the circuit is programmed for a supply voltage of $=0.3V$, we do not need to reprogramme if we switch the supply voltages to $V_{dd} = 0.8V$. The corresponding programming voltage of rail $V_-$ is shown in figure 2.16.

If we look more closely at figure 2.16 we notice the breakpoint of the curves, this is when the output of the circuits converges to $V_{dd}/2$ during UV-programming. At this point the n-MOS is stronger than the p-MOS and to compensate we do have to make the p-MOS stronger. Figure 2.15 shows that the programming of the circuit is linear.

The difference in the characteristic between supply voltage $V_{dd} = 0.8V$, $V_{dd} = 0.5V$ and $V_{dd} = 0.3V$ in figure 2.16 is expected, because the floating-gate on the p-MOS is relative to $V_{dd}$ not to $V_{ss}$. The difference between $V_{dd} = 0.3V$ and $V_{dd} = 0.5V$ is approximately $0.3V$, and between $V_{dd} = 0.5V$ and $V_{dd} = 0.8V$ it is $0.4V$. 

Figure 2.14: Measured n-MOS current $I_n$ of the analog inverter
Figure 2.15: *Measured equilibrium current of the analog inverter*

Figure 2.16: *Measured programming voltage of the analog inverter*
2.4.3 Analog inverter with bias control

Let us then focus at another circuit, the analog inverter with bias control, which is explained in chapter 3. The n-MOS current $I_{ni}$ and $I_{nr}$, with increasing programming voltage $V_{ss}$, are shown in figure 2.18. As the figure 2.17 shows, this is also a symmetrical circuit, with input capacitors $C_{pi}$, and $C_{ni}$, and feedback capacitors $C_{pr}$, and $C_{nr}$. The circuit is implemented with the same U-shaped transistors that has been used in the digital inverter and the analog inverter, $l = 0.6\mu m$ and $w = 10\mu m$, but with the input capacitors $C_{pi} = C_{ni} = 18.4fF$, and feedback capacitors $C_{pr} = C_{nr} = 6fF$ and the bias capacitors $C_b = 14.2fF$.

When looking at figure 2.18, with a supply voltage of 0.8V, the equilibrium current on the input stage $I_{ni}$ is equal to equilibrium current $I_{nr}$, when the programmed supply rail $V_+ = 2.8V$. This gives us a equilibrium current of approximately $0.5nA$. The input stage is similar to a digital inverter and the output stage is an analog diode coupled stage similar to the analog inverter. From the measurement on the equilibrium current in the digital inverter versus the analog inverter, we have seen that the digital inverter will have a higher equilibrium current, however, the difference between equilibrium current on the input and output stage is not as significant, as we should suppose. This is what we have experienced with the measurement on the fabricated chip, and what we have to look more closely to, in a further investigation of this UV-programming process.

If we are looking at the characteristics for $V_{dd} = 0.5V$, we do notice that $I_{ni}$ is equal to $I_{nr}$ when $V_+ = 2.5V$. This gives a equilibrium current $I_{bec} = 0.05nA$. As we should expect the current $I_{ni}$ is larger than $I_{nr}$, and the same is the case with a supply voltage of 0.3V. The respective programming voltage of the supply rail $V_-$ is shown in figure 2.19.

If we focus at the difference of the two n-MOS currents $I_{ni}$ and $I_{nr}$, there is no
significant difference, this means that this circuit is easy to control in respect of the equilibrium current.

The relationship between the equilibrium current $I_{bec}$ and the programming voltage $V_{ss}$ is linear. If we wanted an equilibrium current $I_{bec}$ at approximately $1\mu A$, the corresponding programming voltage $V_{-}$ would be approximately $5V$. 

Figure 2.18: Measured equilibrium current of the analog inverter #2
2.5 Difference in Programming of the Circuits

A circuit in FGUV MOS design will consist of different building blocks, and as we have seen from the measured result on the analog and the digital inverter, they need different programming voltage, figure 2.20. We have to focus this problem more closely. Perhaps we should make transistors with a different geometry in the different blocks, or we could make the UV-hole differently in an analog and a digital inverter. The UV-programming time is approximately the same in the building blocks.

Figure 2.19: *Measured programming voltage of the analog inverter #2*
Figure 2.20: Measured equilibrium current $I_{bec}$

Figure 2.20 shows the different equilibrium current $I_{bec}$, with a supply voltage of 0.5V. Assuming we are using this circuit in weak to moderate inversion, hence equilibrium current is $1nA$ to $1\mu A$. This gives the digital inverter a programming voltage $V_+1$ to $2.4$ V, and of the analog inverter gives $V_+$ between $2.3$ to $3.4$ V, and with the analog inverter #2 the programming voltage $V_+$ is $3.1$ to $5.0$ V. This means, if we are building an amplifier with a digital inverter and a analog inverter, we are able to use a programming voltage $V_+$ from $2.3$ V to $2.4$ V.

Between a digital inverter and an analog inverter #2 there is no intersection, the best solution is separate supply. And finally between an analog inverter and the analog inverter #2 the programming voltage $V_+$ should be $3.1$ V to $3.4$ V.
Chapter 3

Analog and Digital Floating-Gate Circuits

3.1 Introduction

This chapter will cover the different circuits used in the FGUV MOS amplifier design. Other fundamental circuits used in a FGUV MOS design, is not covered in this thesis [15] [29]. In order to make it easier to understand, there will be used some symbols. The symbols are shown in figure 3.1.

![Symbols used in FGUV MOS design](image)

Figure 3.1: Symbols used in FGUV MOS design
3.2 Building Blocks in the FGUV MOS Amplifier Design

3.2.1 Inverters

The inverter is a digital circuit and one of the most fundamental blocks in the FGUV MOS design. This is a useful building block, both in the analog and in the digital circuit. Figure 3.2 shows two kinds of inverters, an one input (a), and a double input inverter (b). The symbols which will be used later in the thesis are shown in figure 3.2 (c).

Inverter - Voltage Characteristics

Figure 3.3 shows the output voltage of the inverter with $V_{dd} = 0.8$ V, $0.5$ V, and $0.3$ V. This is a rail-to-rail signal even with a supply voltage of $0.3$ V. We also notice a reduced gain with $V_{dd} = 0.3$ V, and when the transistors are in strong inversion, hence equilibrium current more than $1 \mu A$.

Figure 3.4 shows the output voltage of a tree row digital inverter structure, with supply voltage $0.5$ V. All digital inverters are implemented with capacitors $C_i = 18.4 fF$, and U-shaped transistors with $l = 0.6 \mu m$ and $w = 10 \mu m$. The measured results in figure 3.4 shows a rail-to-rail output swing for each of the three outputs. The offset between the outputs, is due to mismatch. The UV-programming balance is done on the first inverter in this chain.

The gain of the different nodes is shown in figure 3.5. As we can see, the gain at node #1 is approximately -1.5, in node #2 it is approximately 4.5 and on the output it is approximately -9.5. The gain increases approximately with a factor 3 through each inverter, however this is not an accurate measurement due to the limited resolution.
3.2. BUILDING BLOCKS IN THE FGUVMOS AMPLIFIER DESIGN

Figure 3.3: Measured output voltage of the inverter

Figure 3.4: Measured output from a row of 3 inverters
Figure 3.5: *Measured gain of the 3 rows inverters*

Figure 3.6, shows the gain of the 12 row inverter chain, with the same transistor used in the three row structure, and with supply voltage 0.8 V. The output voltage characteristics are shown in figure 2.9, and 2.10. The inverter has a large gain, and it is useful as an output stage in an analog amplifier design.

**Inverter - Current Characteristics**

The current in the p-MOS transistors of the inverter in figure 3.2 (a) is given by:

\[ I_p = I_{bec}\exp\left\{ \frac{k_i}{nU_T} (V_{dd}/2 - V_{in}) \right\} \]  \hspace{1cm} (3.1)

and similar the current in the n-MOS transistor is:

\[ I_n = I_{bec}\exp\left\{ \frac{k_i}{nU_T} (V_{in} - V_{dd}/2) \right\} \]  \hspace{1cm} (3.2)

If looking at the 2 input inverter in figure 3.2 (b), we can express the p-MOS current by:

\[ I_{pa} = I_{bec}\exp\left\{ \frac{k_i}{nU_T} (V_{dd} - V_{in1} - V_{in2}) \right\} \]  \hspace{1cm} (3.3)

And the n-MOS current is given by:

\[ I_{na} = I_{bec}\exp\left\{ \frac{k_i}{nU_T} (V_{in1} + V_{in2} - V_{dd}) \right\} \]  \hspace{1cm} (3.4)
We name the double input inverter, an additive inverter [14].

The output current of an inverter is sinh shaped as focused in figure 3.7, and the output current is given by:

\[ I_{out} = I_n - I_p = 2I_{bec}\sinh\left\{ \frac{k_i}{nU_T} (V_{in} - \frac{V_{dd}}{2}) \right\} \]  (3.5)

And similar we will get the output current of the double input inverter:

\[ I_{out} = I_{na} - I_{pa} = 2I_{bec}\sinh\left\{ \frac{k_i}{nU_T} (V_{in1} + V_{in2} - V_{dd}) \right\} \]  (3.6)

To use an inverter-chain to increase the gain on the output, is not very useful. We could have used larger input capacitors and longer transistors, or we could use a bias control, on the output stage, as shown in figure 3.8.

The output current on the inverter with bias control is given by:

\[ I_{out} = I_{na} - I_{pa} = 2I_b\sinh\{(V_{in1} + V_{in2} - V_{dd})K\} \]  (3.7)

where \( I_b = I_{bec}\exp(K_b(V_b \frac{V_{dd}}{2})) \), \( K_b = \frac{k_i}{nU_T} \) and \( K = \frac{k_i}{nU_T} \).
Figure 3.7: Measured output current of an inverter with $V_{dd} = 0.8V$

Figure 3.8: Output stage with bias
3.2. BUILDING BLOCKS IN THE FGUVMOS AMPLIFIER DESIGN

3.2.2 Analog Inverters

Two different types of analog inverters [9] [8] [16] are shown in figure 3.9. The analog inverter in (b) is a four transistor symmetric circuit, as we do see the input stage is similar to an inverter, and the output stage is a diode coupled stage. Figure (a) shows a more compact design with only two transistors. The output gain of the circuit in figure (a), is controlled by the capacitive division factor \(k_i\) and \(k_r\), and if we make \(k_r\) a little smaller than \(k_i\), we are able to compensate for the early effect. The output characteristics, both simulated\(^1\) and measured, is shown in figure 3.10. With \(k_r\) smaller than \(k_i\), the gain of the circuit is -1.

\[
\begin{align*}
I_n &= I_{bec} \exp\left\{\frac{1}{nU_T}(V_{in} - V_{dd}/2)k_i\right\} \times \exp\left\{\frac{1}{nU_T}(V_{out} - V_{dd}/2)k_r\right\} \\
I_p &= I_{bec} \exp\left\{\frac{1}{nU_T}(V_{dd}/2 - V_{in})k_i\right\} \times \exp\left\{\frac{1}{nU_T}(V_{dd}/2 - V_{out})k_r\right\}
\end{align*}
\]

Figure 3.9: Analog Inverters

If looking at the analog inverter in figure 3.9 (a) the current \(I_n\) is given by:

\[
I_n = I_{bec} \exp\left\{\frac{1}{nU_T}(V_{in} - V_{dd}/2)k_i\right\} \times \exp\left\{\frac{1}{nU_T}(V_{out} - V_{dd}/2)k_r\right\}
\]

Similar we get the current \(I_p\):

\[
I_p = I_{bec} \exp\left\{\frac{1}{nU_T}(V_{dd}/2 - V_{in})k_i\right\} \times \exp\left\{\frac{1}{nU_T}(V_{dd}/2 - V_{out})k_r\right\}
\]

We let \(I_n = I_p\) and assuming that \(k_i = k_r = k\) this gives:

\[
\begin{align*}
\exp\left\{\frac{k}{nU_T}(V_{in} - V_{dd}/2)\right\} + \exp\left\{\frac{k}{nU_T}(V_{out} - V_{dd}/2)\right\} &= \exp\left\{\frac{k}{nU_T}(V_{dd}/2 - V_{in})\right\} + \exp\left\{\frac{k}{nU_T}(V_{dd}/2 - V_{out})\right\} \\
\exp\left\{\frac{k}{nU_T}(V_{in} + V_{out} - V_{dd})\right\} &= \exp\left\{\frac{k}{nU_T}(V_{dd} - V_{in} - V_{out})\right\}
\end{align*}
\]

If we solving this for \(V_{out}\) it gives, \(V_{out} = V_{dd} - V_{in} \equiv V_{in}^*\), which is an analog inverted input signal, with gain -1.

\(^1\)Simulation is done with SpectreS, which is included in the Cadence applications program.
Figure 3.10: *Simulated and measured data of the analog inverter*

Figure 3.11: *Measured output voltage of the analog inverter #1*
3.2. **BUILDING BLOCKS IN THE FGUVMS AMPLIFIER DESIGN**

The analog inverter \#1 is implemented in the AMS 0.6μ process [1] using transistors with \( w = 10\mu \), \( l = 0.6\mu \) and \( C_i = 18.4fF \), \( C_r = 14.2fF \). The analog inverter may be programmed to different supply voltages, \( V_{dd} \). The measured results of supply voltages \( V_{dd} = 0.3V \), \( V_{dd} = 0.5V \), and \( V_{dd} = 0.8V \) is shown in figure 3.11. The linear range of operation, for extreme low supply voltages is limited by the linear region of the transistor, approximately \( 4U_T \) in weak inversion.

**Analog Inverter - Output Characteristics with \( V_{dd} = 0.8V \)**

The analog inverter can operate in weak inversion, through moderate to strong inversion. Hence equilibrium current, \( I_{bec} \) from 0.4nA to 2.0μA, as we can see of the output voltage in figure 3.11. The output signal is almost rail-to-rail, it is 13.5mV from \( V_{ss} \) and 40mV from the \( V_{dd} \). This gives an output voltage amplitude of 746.5 mV.

As long as the equilibrium current, \( I_{bec} \) is less than 1μA, the output voltage is almost analog inverting the input, hence the gain is -1. With \( I_{bec} \) more than 1μA, the transistors are in strong inversion, and the output voltage is not perfectly analog inverted, the gain is less than -1.

![Measured analog inverter gain](image)

**Figure 3.12:** *Measured output gain versus \( I_{bec} \) of the analog inverter \#1*

If we are increasing the equilibrium current, we get less gain as shown in figure 3.12. This can be explained when the transistors are going from weak inversion to strong inversion. The gain is decreased when the output is getting closely to the supply rails, due to the linear region of the transistors.
Figure 3.13: Measured gain of the analog inverter #1

Figure 3.13 shows the gain of the analog inverter. As we can see the linear region of the gain is 0.1V to 0.65V.

**Analog Inverter - Output Characteristics with \( V_{dd} = 0.5V \)**

Figure 3.11 shows the output voltage of the analog inverter with \( V_{dd} = 0.5V \), and equilibrium current from 0.14\( nA \) to 300\( nA \). The output swing is 42mV from \( V_{dd} \) and 6mV from the \( V_{ss} \), which is almost rail-to-rail, and output voltage amplitude is 452mV.

The linear region of the gain as shown in figure 3.13, is 0.15V to 0.37V with supply voltage of 0.5V.

**Analog Inverter - Output Characteristics with \( V_{dd} = 0.3V \)**

The output voltage of the analog inverter with the supply voltage of 0.3 V, is just shown with equilibrium current from 0.1\( nA \) to 0.4\( nA \). The output swing is 45mV from \( V_{dd} \) and 7mV from the \( V_{ss} \), which gives the output voltage of 248mV.

The linear region of the gain is 0.15V to 0.2V as shown in figure 3.13.

**The Quality of a Analog Inverter**

If focusing on figure 3.14, we do notice that the analog inverter are able to operate from weak inversion through moderate to strong inversion, hence equilibrium current
3.2. BUILDING BLOCKS IN THE FGUVMS AMPLIFIER DESIGN

$I_{bec}$ from 0.4nA to 2μA, with $V_{dd} = 0.8$V, then the gain is from -1.01 to -0.93. With a power supply of 0.5 V and equilibrium current ranging from 0.1nA to 1μA, the gain is from -0.99 to -0.89.

![Figure 3.14: Measured gain versus $I_{bec}$ of the analog inverter #1](image)

**The Output Current of an Analog Inverter**

If we combine equation 3.8 and 3.9, and assuming $k_i = k_r = k$, we get the output current:

$$I_{out} = I_n - I_p = 2I_{bec} sinh\{K(V_{in} + V_{out} - \frac{V_{dd}}{2})\}$$

where $K = \frac{k}{nU_T}$. The output current is $sinh$ shaped, which gives the same shape as the output current of an inverter, as the measured output current shows in figure 3.15. This means that the circuit can be used either as an input stage or as an output stage. If we are using it as an output stage, we can add a bias control. The output current is then given by:

$$I_{out} = I_n - I_p = 2I_b sinh\{K(V_{in} + V_{out} - \frac{V_{dd}}{2})\}$$

where $K = \frac{k}{nU_T}$ and $I_b = I_{bec} exp\{\frac{k}{nU_T}(\frac{V_{dd}}{2} - V_b)\}$. 
3.2.3 The Floating-Gate Analog Inverter #2

The floating-gate analog inverter \([10]\) in figure 3.16 is made of four transistors and have a bias control voltage input. The analog inverter #2 is implemented with \(C_i = 18.4fF\), \(C_r = 6fF\). The transistors are U-shaped with \(l = 0.6\mu m\) and \(w = 10\mu m\).

The input stage is a digital inverter, and therefore the currents on the input stage in figure 3.16 are given by:

\[
I_{pi} = I_{bec} \exp\left(\frac{k_i}{nU_T}(V_{dd} - V_{in1})\right) \tag{3.12}
\]
\[
I_{ni} = I_{bec} \exp\left(\frac{k_i}{nU_T}(V_{in1} - V_{dd})\right) \tag{3.13}
\]

And the output stage is a linear output stage also called a diode coupled stage, and the current can be expressed as:

\[
I_{pr} = I_{bec} \exp\left(\frac{k_r}{nU_T}\left(\frac{V_{dd}}{2} - V_{out}\right)\right) \tag{3.14}
\]
\[
I_{nr} = I_{bec} \exp\left(\frac{k_r}{nU_T}(V_{out} - \frac{V_{dd}}{2})\right) \tag{3.15}
\]
3.2. BUILDING BLOCKS IN THE FGUMOS AMPLIFIER DESIGN

![Diagram of the floating-gate analog inverter #2]

Figure 3.16: The floating-gate analog inverter #2

**Analog Inverter #2 - The Output Characteristics with** $V_{dd} = 0.8V$

Figure 3.17 shows the output voltage of the analog inverter with equilibrium currents from 4.8nA to 98nA.

When the equilibrium current is small, the n-MOS does not work properly, and it is not pulling all the way to the rail. When the equilibrium current is more than 30nA the output swing is almost rail-to-rail, it is approximately 10mV from the $V_{dd}$ and $V_{ss}$ supply rails. This gives an output voltage swing of 780mV.

The output gain and linearity is controlled by the capacitive division factor $k_i$ and $k_r$, by using a slightly smaller $k_r$ we can compensate for the Early effect. If we do change the capacitive division factor $k_i$ and $k_r$ we will be able to change the gain. We have $I_{p1} + I_{pr} = I_{ni} + I_{nr}$, assuming $k_r = 3k_i$. It gives the output voltage $V_{out} = \frac{V_{in}}{3}$.

Figure 3.18, shows the output current with increasing equilibrium current from 4.8nA to 98nA. The maximum output current $I_{out}^{max}$, with equilibrium current $I_{bec} = 98nA$, is 2.8μA, and with equilibrium current $I_{bec} = 4.8nA$ the $I_{out}^{max}$ is 0.25μA.
Figure 3.17: *Measured output voltage of the analog inverter #2, $V_{dd} = 0.8V$*

Figure 3.18: *Measured output current of the analog inverter #2, $V_{dd} = 0.8V$*
3.2. BUILDING BLOCKS IN THE FGUVMS AMPLIFIER DESIGN

Figure 3.19 shows the transconductance $G_m$. We can see transconductance is increasing when approaching the supply rails. This is an interesting feature of a $\text{sinh}$ amplifier, because traditional amplifier has a $\text{tanh}$ shaped current, where the transconductance decreases due to transistors operating in the linear region.

When looking at the relative transconductance shown in figure 3.20, the equilibrium current is in a range from $0.14nA$ to $120nA$, we do notice with increasing equilibrium current $I_{bec}$, the output current is getting more linear, since the transistors are in strong inversion.

Figure 3.19: Measured transconductance ,$V_{dd} = 0.8V$
Figure 3.20: Measured relative transconductance, $V_{dd} = 0.8V$

**Analog Inverter #2 - The Output Characteristics with $V_{dd} = 0.5V$**

Figure 3.21 shows the output voltage with equilibrium current from $1.4nA$ to $130nA$. With a too small equilibrium current the voltage output swing is not rail-to-rail, it is not pulling all the way to the rails. For an optimal equilibrium current, the output reaches within $10mV$ from each rails, this gives an output voltage swing of $480mV$.

The figure 3.22 shows the output current $I_{out}$ with equilibrium current from $1.4nA$ to $130nA$. The maximum output current $I_{out}^{max}$ is $1.6μA$ with equilibrium current $I_{bec} = 130nA$, and the $I_{out}^{max}$ is $40nA$ with an equilibrium current $I_{bec} = 1.4nA$. 
3.2. BUILDING BLOCKS IN THE FGUV MOS AMPLIFIER DESIGN

Figure 3.21: Measured output voltage of the analog inverter #2, \( V_{dd} = 0.5V \)

Figure 3.22: Measured output current of the analog inverter #2, \( V_{dd} = 0.5V \)
Figure 3.23 shows the transconductance of the analog inverter with equilibrium current from 0.06nA to 74nA. We do notice the transconductance is decreased compared to supply voltage of $V_{dd} = 0.8V$.

![Transconductance Gm of the additive analog inverter (Vdd=0.5 V)](image)

Figure 3.23: *Measured transconductance, $V_{dd} = 0.5V$*

Since the output current is less sinh shaped, the relative transconductance is more ideal as seen in figure 3.24, hence the output current is more linear.


Figure 3.24: Measured relative Transconductance, $V_{dd} = 0.5V$

Analog Inverter #2 - The Output Characteristics with $V_{dd} = 0.3V$

Figure 3.25 shows the output voltage with equilibrium current from 0.6nA to 68nA.

When the equilibrium current is to small, the voltage output is not rail-to-rail, we need a certain equilibrium current to achieve an optimal voltage output swing. The output reaches within 17mV from $V_{dd}$ and 15mV from $V_{ss}$ for a optimal equilibrium current, this gives an output voltage swing of 268mV. The reason why we do not get an optimal output swing, is because the transistors are reaching the linear region of operation.

Figure 3.26 shows the output current $I_{out}$, with equilibrium current from 0.6nA to 68nA. The maximum output current $I_{out}^{max}$ is 0.5μA with equilibrium current $I_{bec} = 68nA$, and $I_{out}^{max}$ is 9nA with equilibrium current $I_{bec} = 0.6nA$. We do notice the $I_{out}^{max}$ is reduced when we are reducing the supply voltage, not surprisingly, since it follows a linear law.
Figure 3.25:  Measured output voltage of the analog inverter #2, $V_{dd} = 0.3V$

Figure 3.26:  Measured output current of the analog inverter #2, $V_{dd} = 0.3V$
Figure 3.27 shows the transconductance of the analog inverter with equilibrium current from 0.05nA to 50nA. The output characteristic is still sinh shaped, and decreased compared to supply voltage of 0.5 V. The circuit is now operating in the linear region.

If looking at the relative transconductance in figure 3.28, we notice that the output current is more linear over the hole range of the equilibrium currents, compared to the other supply voltages.
3.2.4 The Floating-Gate Additive Analog Inverter with Tunable Gain

The Floating-Gate analog additive inverter [17] [8] [14] is an analog inverter with double inputs, figure 3.29. And it does also have a tunable gain or bias control. The input stage is a two input digital inverter, and then the currents on the input stage in figure 3.29 is given by:

\[ I_{pi} = I_b \exp\left\{ \frac{k_i}{nU_T} (V_{dd} - V_{in1} - V_{in2}) \right\} \]  
\[ I_{ni} = I_b \exp\left\{ \frac{k_i}{nU_T} (V_{in1} + V_{in2} - V_{dd}) \right\} \]

where the bias current \( I_b \) is:

\[ I_b = I_{bec} \exp\left\{ \frac{k_b}{nU_T} (V_b - V_{dd}/2) \right\} \]

The output stage is diode coupled, and the current may be expressed as:

\[ I_{pr} = I_{b}^* \exp\left\{ \frac{k_r}{nU_T} \left( \frac{V_{dd}}{2} - V_{out} \right) \right\} \]
\[ I_{nr} = I_{b}^* \exp\left\{ \frac{k_r}{nU_T} \left( V_{out} - \frac{V_{dd}}{2} \right) \right\} \]
where the bias current $I_b^*$ is:

$$I_b^* = I_{bec} \exp \left( \frac{k_b}{nU_T} (V_{dd}/2 - V_b) \right)$$

The additive analog inverter is implemented with $C_i = 18.4fF$, $C_r = 6fF$ and $C_b = 14.2fF$. The transistors U-shaped with $l = 0.6\mu m$ and $w = 10\mu m$. Figure 3.2.4 shows the output voltage of the additive analog inverter both simulated and measured. As we can see, we have a gain less than -1, obviously since $C_i$ is larger than $C_r$, the bias voltage is set to $V_{dd}/2$.

Figure 3.3.1 shows the effect of the bias control voltage, $V_b$ from 0 to 0.8V with two equilibrium currents $I_{bec1} = 17nA$ (dotted) and $I_{bec2} = 100nA$ (solid). The supply voltage is 0.8V, and the voltage input $V_{in2} = V_{dd}/2$. We do notice that the dynamic range of the output voltage or the gain of the circuit, controlled by the bias voltage, is decreased with increasing $I_{bec}$.

The output characteristics of the output current with two equilibrium currents $I_{bec1} = 17nA$ (dotted) and $I_{bec2} = 100nA$ (solid) and with supply voltage of 0.8V, is shown in figure 3.3.2. If we do increase the equilibrium current $I_{bec}$, the maximum output current, $I_{out}^{max}$, is increased, hence with increasing equilibrium current $I_{bec}$, the gain is decreased and output current $I_{out}$ is increased.
Figure 3.30: Simulated and measured data of the analog additive inverter

Figure 3.31: Measured output voltage of the additive analog inverter with two \( I_{\text{bec}} \) currents and bias control, \( V_{\text{dd}} = 0.8V \)
The Analog additive inverter with $V_{dd} = 0.8V$

The output characteristics of the additive analog inverter with bias is, shown in figure 3.33. If we focus at the voltage swing on the output $V_{out}$, we will see that this is a proper rail-to-rail amplifier, the output is 2$mV$ from $V_{dd}$ and 1$mV$ from $V_{ss}$. This gives a voltage amplitude of 797$mV$, or 99.6 % output signal.

The figure 3.34, shows the relationship between the output gain and the bias voltage. With the bias control it is possible to adjust the gain and linearity. The dynamic range of the gain is dependent of the equilibrium current, as showed in figure 3.34. With a equilibrium current of $5nA$ the gain is adjustable from 0 to -3.6, with the equilibrium current at $100nA$ the range is from -0.1 to -3.2. We notice, we do have a larger dynamic range when the equilibrium current is small, this due to the increasing equilibrium current, hence the transistors are approaching strong inversion.

The normalized transconductance of the additive analog inverter, is shown in figure 3.35. As mentioned earlier it is possible to adjust the linearity of the circuit with the help of bias control. The normalized transconductance $G_m$ shows the relationship between bias and linearity, with the increasing bias voltage the output current is more linear.
CHAPTER 3. ANALOG AND DIGITAL FLOATING-GATE CIRCUITS

Figure 3.33: Measured output voltage of the additive analog inverter with bias control, $V_{dd} = 0.8V$

Figure 3.34: Measured gain of the additive analog inverter with bias control, $V_{dd}=0.8V$. 
The Analog additive inverter with $V_{dd} = 0.5V$

The output characteristics of the additive analog inverter with bias, is shown in figure 3.36. If looking at the voltage swing on the output $V_{out}$ we will see, this is a real rail-to-rail amplifier, it is 5$mv$ from $V_{dd}$ and 2$mv$ from $V_{ss}$, this gives a voltage amplitude swing of 493$mV$, or 98.6 % output signal.

Figure 3.37 shows the gain with increasing bias voltage. With equilibrium current $I_{bec} = 0.5nA$ the gain is in the variability between -0.1 to -2.1, and when the equilibrium current $I_{bec}$ is 130$nA$, the gain is -1.7 to -0.25. If we compare these results with the supply voltage of 0.8 $V$, we will observe a reduction in the dynamic range. We do notice when the equilibrium current is increasing, the transistors going towards strong inversion, hence the bias voltage adjustment will not affect the output voltage in the same amount.

The normalized transconductance of the additive analog inverter is shown in figure 3.38. The output current is more linear compared to supply voltage 0.8 $V$. 

---

**Figure 3.35:** Measured normalized transconductance of the additive analog inverter
Figure 3.36: Measured output voltage of the additive analog inverter with bias control, $V_{dd} = 0.5V$

Figure 3.37: Measured gain of the additive analog inverter with bias control, $V_{dd} = 0.5V$
3.2. BUILDING BLOCKS IN THE FGUVMOS AMPLIFIER DESIGN

The Analog additive inverter with $V_{dd} = 0.3V$

The output characteristics of the additive analog inverter with bias, is shown in figure 3.39. The voltage swing on the output $V_{out}$ is almost rail-to-rail, it is 10$mV$ from $V_{dd}$ and 8$mV$ from $V_{ss}$, which gives a voltage amplitude of 282$mV$, this is 94% voltage output swing.

Let us then focus how the equilibrium current affects the gain. When $I_{bec} = 0.3nA$ the gain is -0.95 to -0.15, and for $I_{bec} = 70nA$ the gain is -0.8 to -0.35, figure 3.40. We do also notice that the dynamic range is decreased with reduced power supply $V_{dd}$, and increased equilibrium current.

The normalized transconductance of the additive analog inverter is shown in figure 3.41. The circuit is more linear with reduced supply voltage.
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Figure 3.39: Measured output voltage of the additive analog inverter with bias control, $V_{dd} = 0.3V$

Figure 3.40: Measured gain of the additive analog inverter with bias control, $V_{dd} = 0.3V$
3.2. BUILDING BLOCKS IN THE FGUV-MOS AMPLIFIER DESIGN

Output Characteristics

From equations 3.16, 3.17, 3.18, 3.19, we have the currents $I_{pi} + I_{pr} = I_{ni} + I_{nr}$, and $V_b = V_{dd}/2$, assuming $k_r = 2k_i$ this gives:

$$V_{out} = \{(V_{in1} + V_{in2})/2\}^* = (V_{dd} - (V_{in1} + V_{in2}))/2$$

We know that the output gain is related to the capacitive division factor $k_i$ and $k_r$. This means that there is a relationship between input capacitor $C_i$ and feedback capacitor $C_r$. As mentioned in section 3.2.3, the capacitive division factor can be utilized to increase the linearity and reduced the gain. If $k_r = 4k_i$ then the output voltage, $V_{out} = \{(V_{in1} + V_{in2})/4\}^*$

The bias inputs $V_b$ and $V_b^*$ provide a dynamic transconductance $G_m$ and linearity control, as shown earlier in figures 3.35, 3.38 and 3.41. In addition figure 3.42 shows, when $V_b \gg V_b^*$, the total output current $I_{out}$ is reduced.

The measured output characteristics of the additive analog inverter with tunable gain are shown in figure 3.43. If $V_b^* \gg V_b$ the output can be approximated by the sinh function:

$$V_{out} \approx V_{dd}/2 \times (1 - sinh\{K(V_{in1} - V_{in2}/2)\})$$

As also shown in figure 3.33, 3.36 and 3.39, where $K$ is inversely proportional to $V_b^*-V_b$, and when $V_b \gg V_b^*$ the output can be approximated by a tanh function:
\[ V_{\text{out}} \approx V_{dd}/2 \times (1 - \tanh\{K'(V_{i1} - V_{i2})/2\}) \]

where \( K' \) is inversely proportional to \( V_b - V_b^* \).

Generally we can then express the output voltage as a function:

\[ V_{\text{out}} = F\{ V_{dd} - (V_{i1} - V_{i2})/2 \} \]

where \( F \) can be a \( \text{sinh} \), \( \text{tanh} \) or a \( \text{linear} \) function depending on the bias control voltage.

![Graph](image)

Figure 3.42: Measured output current of the additive analog inverter

**Summary of the additive Analog Inverter**

With the bias voltage \( V_b \) and \( V_b^* \) we are able to make a dynamic transconductance \( G_m \) control, or we can change the output voltage characteristic. The gain can be adjust with bias control or by changing the input capacitance \( C_i \) and the feedback capacitor \( C_r \). Even if we are using a supply voltage as low as 0.3 V, we do still have a amplifier (OTA), which have almost rail-to-rail performance.

The additive analog inverter is a building block with several opportunities, because of the tuning ability. It is possible to use it as a stand alone amplifier, or as a linearizing element in an OTA design.
3.2. BUILDING BLOCKS IN THE FGUVMOS AMPLIFIER DESIGN

3.2.5 Floating Gate Current Sum Circuit

The Floating-Gate current sum is a building block used in the OTA design of making a Tanh-amplifier [13], which will have a tanh shaped output current. All of the previous blocks have a sinh shaped output current, hence we call them Sinh-amplifiers. This is not a stand alone circuit. The Tanh-amplifier will be discussed in section 4.3.

We have two kinds of current sum circuits [13], it is a n-MOS and a p-MOS input circuit as shown in figure 3.44.

The output current $I_p$ of the p-MOS circuit is given by:

$$I_p = I_{n1} + I_{n2}$$

$$\exp\left(\frac{k_r}{nU_t} \left( \frac{V_{dd}}{2} - V_{out} \right) \right) = \exp\left(\frac{k_r}{nU_t} \left( V_1 - \frac{V_{dd}}{2} \right) \right) + \exp\left(\frac{k_r}{nU_t} \left( V_2 - \frac{V_{dd}}{2} \right) \right)$$

And similarly the output current of the n-MOS circuit $I_n$ is:

$$I_n = I_{p1} + I_{p2}$$

$$\exp\left(\frac{k_r}{nU_t} (V_{out} - \frac{V_{dd}}{2}) \right) = \exp\left(\frac{k_r}{nU_t} \left( \frac{V_{dd}}{2} - V_1 \right) \right) + \exp\left(\frac{k_r}{nU_t} \left( \frac{V_{dd}}{2} - V_2 \right) \right)$$
CHAPTER 3. ANALOG AND DIGITAL FLOATING-GATE CIRCUITS

(a) N-Type  (b) P-Type  (c) Symbols

Figure 3.44: The Floating Gate Current Sum Circuits

Figure 3.45: Simulated results of the P-Type Floating Gate Current Sum Circuits
Chapter 4

The Ultra Low Voltage FGUVMOS Amplifier

4.1 Introduction

This chapter provides some examples of different amplifying circuits implemented with FGUVMOS transistors. All circuits consist of U-shape transistors with \( l = 0.6 \mu m \) and \( w = 10 \mu m \). The typical gate capacitance \( C_g \) of this kind of transistor is approximately 14 fF, hence the total input capacitance \( C_i \) should not be less than \( C_g \).

The designed FGUVMOS circuits will be Operational Transconductance Amplifiers (OTA), also called a transconductance element, as it converts a voltage input to a current output. This gives:

\[
I_{out} = G_m V_{in}
\]

If we look at the difference between an Op-amp and an OTA, an Op amp has a very high open-loop gain, and uses feedback to guarantee a linear operation over a wide range of operation [23]. A OTA uses no external feedback and their transfer and impedance functions are directly dependent on the \( G_m \) in the OTA.

4.1.1 DC - Characteristics

The previous chapters have presented the DC-characteristics of the different building blocks, and by connecting these different building blocks together, we expect the circuits to be working properly. We have seen that FGUVMOS circuits are rail-to-rail amplifiers with a low supply voltage, hence they will have a suitable dynamic range even for supply voltages below 1 Volt.
4.1.2 AC - Characteristics

Bandwidth, Gain, and Phase response

A transconductance ($g_m$) stage converts the small-signal-differential input voltage, into a current[18]. The formula for the small signal $g_m$ is given by:

$$g_m = \frac{q}{kT} I_b$$

where $\frac{q}{kT} = \frac{1}{26mV}$ $q$ is the electron charge and $k$ is Boltzmann’s constant, $I_b$ is the bias current and $T$ is absolute temperature. At $+25^\circ C$, $V_T = \frac{kT}{q} = 26mV$ and $VT$ is the thermal voltage.

The low frequency breakpoint of the amplifier $f_o$ is given by:

$$f_o = \frac{1}{2\pi R_o C_p}$$  \hspace{1cm} (4.1)

where $R_o$ is the output impedance and $C_p$ is the dominant pole capacitance.

The high frequency response is determined by $g_m$ and $C_p$

$$V_{out} = V_{diff} \frac{g_m}{j\omega C_p}$$

The unity gain-bandwidth$^1$ frequency, $f_u$ is given when $|V_{out}| = |V_{diff}|$ and gives:

$$f_u = \frac{g_m}{2\pi C_p}$$  \hspace{1cm} (4.2)

As we can see in equation 4.2, if we compare the transconductance $g_m$ of a sinh and a tanh amplifier we know that a sinh amplifier has increasing $g_m$ when it is reaching the supply rails, hence the the sinh OTA has better frequency response when it is reaching the rails than a tanh OTA.

The amplification of a circuit, or also called the gain, is given by:

$$G_{\text{gain}} = 20\log \frac{U_{out}}{U_{in}}$$

This is also known as the voltage gain of the circuit. The cutoff frequency $f_c$, is given when the voltage gain is -3 dB. The FGUVMOS amplifiers (OTA) in this thesis is specified with open loop gain.

The phase response of a circuit describes the stability of the circuit. An oscillator has a phase shift of 180$^\circ$, between input and output. We have to make sure that if we are going to make an amplifier, the phase margin has to be less than -180$^\circ$ at the frequency $f_u$, if not we will have an oscillation.

$^1$The unity gain-bandwidth is at the point where the open loop gain is unity.
4.1. INTRODUCTION

Harmonic Distortion

Harmonic distortion is distortion caused by the presence of frequencies that are not present in the input signal. Total harmonic distortion (THD) of a signal, is the ratio of the sum of the powers of all harmonic frequencies above the fundamental frequency to the power of the fundamental frequency.

The constructed Sinh OTA’s are more linear than tanh OTA’s, typical values of the different OTA’s is shown in the table. A way of making the FGUVMOS circuits more linear is by using the bias voltage. If we look at the relative transconductance we can increase the linear region, with adjusting the bias current $I_b$. If we could be able to make combinations of a sinh OTA and a tanh we could make an even better linear amplifier, hence reducing the harmonic distortion.

<table>
<thead>
<tr>
<th>Type #</th>
<th>Description</th>
<th>Linear range</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Tanh</td>
<td>30 – 50mV</td>
</tr>
<tr>
<td>2</td>
<td>Sinh</td>
<td>50 – 80mV</td>
</tr>
<tr>
<td>3</td>
<td>Tanh+Sinh</td>
<td>150 – 250mV</td>
</tr>
<tr>
<td>4</td>
<td>Sinh(Tanh)</td>
<td>200 – 300mV</td>
</tr>
</tbody>
</table>

$^2$Harmonic distortion is caused by nonlinearities within the device.

$^3$The THD is usually expressed in dB. Measurements for calculating the THD are made at the output of a device under specified conditions.
4.2 OTA with Floating-Gate Circuits

4.2.1 The Simple Differential Amplifier

By using an analog inverter and a double input inverter, it is possible to obtain a simple differential amplifier [2]. The input stage consists of an analog inverter which has the characteristics covered in the previous chapter, and the output stage is a double input inverter with or without bias control. The amplifier is shown in figure 4.1. Figure 4.2 gives more detail look of the amplifier.

The circuit is simulated with $C_i = C_p = C_n = 18.5fF$ and $C_r = 15fF$. The transistors are U-shaped with AMS 0.6 process parameters and $l = 0.6\mu m$ and $w = 10\mu m$. 
If looking at the amplifier without bias control, the output current is:

\[ I_{\text{out}} = I_p - I_n \]
\[ = I_{\text{bec}} \exp \left( \frac{k_i}{nU_t} (V_{dd} - V_{in1^*} - V_{in2}) \right) - \exp \left( \frac{k_i}{nU_t} (V_{in1^*} + V_{in2} - V_{dd}) \right) \]
\[ = 2I_{\text{bec}} \sinh \left( \frac{k_i}{nU_t} (V_{dd} - V_{in1^*} - V_{in2}) \right) \]

if substituting \( V_{in1^*} = V_{dd} - V_{in1} \), we get the output current:

\[ I_{\text{out}} = 2I_{\text{bec}} \sinh \left( \frac{k_i}{nU_t} (V_{in1} - V_{in2}) \right) \]

If we are using the output stage with bias control, the output current is:

\[ I_{\text{out}} = 2I_b \sinh \left( \frac{k_i}{nU_t} (V_{in1} - V_{in2}) \right) \]

where \( I_b = I_{\text{bec}} \exp \left( \frac{k_i}{nU_t} (V_b - \frac{V_{dd}}{2}) \right) \).

The simple differential amplifier is a OTA with a sinh shaped output current, hence it gives a transconductance which is increasing when it is reaching the supply rails.

Figure 4.3 shows the simulated frequency response with equilibrium current \( I_{\text{bec}} \) approximately 60\( \mu \)A. The voltage gain of the circuit is approximately 20 dB. The frequency response is 3 MHz (+0/-3dB), with the phase shift of 55\(^\circ\), and the roll-off response is 20dB/decade which gives one dominant pole. The Unity Gain Bandwidth (GBW) is 11 MHz and phase shift is -110\(^\circ\), which makes this amplifier design stable. The phase response is shown in figure 4.4.

As we can see, it is possible to make a very simple fully functional differential amplifier with the use of only four transistors.
Figure 4.3: Simulated frequency response of a simple differential amplifier

Figure 4.4: Simulated phase response of a simple differential amplifier
4.2. OTA WITH FLOATING-GATE CIRCUITS

4.2.2 The Sinh Amplifier differential in and outputs

Differential amplifier with bias

A transconductance amplifier with differential in and output is a very useful circuit in analog design, for instance if we are going to build a filter section, or if we need a balanced input or output stage. The sinh amplifier in figure 4.5 has differential outputs and inputs. The implemented amplifier is shown in figure 4.6. It consists of an analog inverter, the additive analog inverter, and the output stage is an inverter. As we can see the additive inverter is with a bias control, and this will be the gain control of the circuit.

![Block diagram of the Sinh amplifier with differential inputs](image1)

**Figure 4.5: Block diagram of the Sinh amplifier with differential inputs**

![Sinh amplifier with differential inputs](image2)

**Figure 4.6: Sinh amplifier with differential inputs**

The amplifier is implemented with the capacitors values seen in figure 4.6. As been
explained in section 2.5, we need different programming voltages for the analog inverter, the additive analog inverter, and the inverter. To make the additive analog inverter to work properly we need a programming voltage larger than 2.7 V applied to $V_{ss}$. Then the inverter on the output is in strong inversion. This means that the drain-source current $I_{ds}$ is larger than $1\mu A$. This is the reason why the bias control circuit does not have an effect on the output voltage, and is not shown.

The output current of the analog additive inverter is given by:

$$I_{out-} = I_b \sinh\left\{ \frac{k}{nU_T} (V_{out-} - V_{dd}) \right\}$$

where $I_b$ is: $I_b = I_{bec} \exp\left\{ \frac{k_b}{nU_T} (V_b - V_{dd}/2) \right\}$ and $k_b$ are the capacitive division factor.

Figure 4.7 shows the output current of the analog additive inverter with increasing equilibrium current, and shows that this stage is working as expected.

The measured output voltage $V_{out-}$ and $V_{out+}$ are shown in figure 4.8 and figure 4.7. The input $V_{in}$, $V_b$, and $V_b^*$ are set to $V_{dd}/2$. If looking at the output current $I_{out+}$ on the output stage, it is given by:

$$I_{out+} = 2I_{bec} \sinh\left\{ \frac{k_i}{nU_T} \left( \frac{V_{dd}}{2} - V_{out-} \right) \right\}$$

(4.3)
4.2. OTA WITH FLOATING-GATE CIRCUITS

We know from the measurement on the additve inverter that the output voltage, seen in equation 3.20, is \( V_{\text{out}} = F(V_{\text{dd}} - V_+ - V_-)/2 \), where \( F \) can be a \( \text{sinh}, \text{tanh} \) or a linear function. If we apply this in equation 4.3, for the output current this gives:

\[
I_{\text{out}+} = 2I_{\text{bec}} \text{sinh} \left( \frac{k_i}{nU_T} \left( \frac{V_{\text{dd}}}{2} - F(V_- - V_+)/2 \right) \right)
\]  

(4.4)

Even if not having optimal working conditions, we are able to make a differential amplifier, the offset in the output is due to mismatch. The gain on the output stage of the amplifier is approximately 16, as shown in figure 4.9. The reason why the gain is not higher is because the equilibrium current on the output stage is more than 10 \( \mu \)A, hence the inverter is in strong inversion, and the gain on the output is decreased, as shown in section 2.4.1.

![Figure 4.8: Measured output voltage of the sinh amplifier](image)

AC measurement on the amplifier is a little difficult to achieve, because the load on the PAD of the designed chip, makes an dominant pole (1. order low pass-filter). The simulated frequency response is shown in figure 4.10. The frequency response is 2 MHz (+0/-3dB), with -80° phase shift. The roll off response is 20 dB/decade and indicates one dominant pole. The Gain Bandwidth is 5 MHz, with -110° phase shift, which indicates a stabil circuit. The total voltage gain is approximately 9 dB. The phase response is shown in figure 4.11.

If looking at the measured output characteristics of the circuit in figure 4.8, we notice the difference in gain of the \( V_{\text{out} -} \) and \( V_{\text{out} +} \), which also was discovered in the simulation of the circuit, hence this is not a good balanced differential output. A way of solving
Figure 4.9: Measured gain of the sinh amplifier

Figure 4.10: Simulated frequency response of the sinh amplifier $Vdd = 0.5 \text{ V}$
this problem is by using an analog inverter on the output, as shown in figure 4.12. 

Figure 4.14 shows the simulated output voltage $V_{out-}$ and $V_{out+}$, and as we do notice this is a proper balanced differential output stage.

If we should increase the total gain of the circuit we could change the gain of the additive analog inverter, hence change relationship between the capacitors $C_i$ and $C_r$ explained in section 3.2.3. As we can see in figure 4.13, input capacitor $C_i$ is $27.1fF$ and feedback capacitor $C_r$ is $6fF$. Another way of increasing the gain on the output stage, is by making the input capacitors on the output stage larger, hence the capacitor $C_{inv}$ is $100fF$, or we could made the transistors longer.

Figure 4.11: *Simulated phase response of the sinh amplifier, $V_{dd}= 0.5 V$*

Figure 4.12: *Block diagram Sinh Amplifier with differential in- and outputs*
CHAPTER 4. THE ULTRA LOW VOLTAGE FGUVMOS AMPLIFIER

Figure 4.13: Sinh Amplifier with differential in - and outputs

Figure 4.14: Simulated output voltage of the sinh Amplifier with differential in - and outputs
The Sinh Follower

Figure 4.15 shows a voltage follower, using the sinh amplifier in figure 4.6.

\[ V_{out} = A(k_i+V_{in+} - k_i-V_{out}) \]  (4.5)

Which gives the following transfer function:

\[ \frac{V_{out}}{V_{in+}} = \frac{k_i+}{1 + k_i-} \]  (4.6)

Where A is the amplification or Gain of the circuit, and \( k_i+ \) and \( k_i- \) is the capacitive division factor on the input \( V_+ \) and \( V_- \) respectively. The gain of this circuit is measured to 16, like what is shown in figure 4.9. When focusing at the transfer function 4.6, we do see if we make the \( K_i+ \) a little larger than \( k_i- \) we are able to make a proper voltage follower.

The simulated result in figure 4.16, shows the expected output characteristic with supply voltage 0.5 V, hence we can make a suitable voltage follower with low supply voltage using FGUVMOS technology. Figure 4.17 shows the offset voltage between in and output of the circuit. The error is approximately 1mV, in the interval from 0.1mv - 499mV or 0.2 %, which is acceptable.
CHAPTER 4. THE ULTRA LOW VOLTAGE FGUVMOS AMPLIFIER

Figure 4.16: Simulated output of the Sinh follower

Figure 4.17: Simulated (Vin - Vout) of the sinh follower
4.2.3 Transconductance amplifier with dynamic load

Another way of designing a fully differential FGUV MOS transconductance amplifier is shown in figure 4.18. This is structure based on the Bram Nauta’s transducer element [20] [12] [29], but this is not exactly similar, since Nauta uses six CMOS inverters, Nauta also used the supply nodes to control the transconductance, and an additional circuit for the bias control.

Since the circuit has no internal nodes, there are no parasitic poles. The analog inverters A_inv3 and A_inv4, are shunted resistance, connected between the output nodes and the common mode voltage $V_{dd}/2$. The value of these resistance is $1/g_{m3}$, and
1/$g_{m4}$ which is the transconductance of the analog inverters. These elements is making the output resistance dynamic. The transconductance are at the maximum for common mode output signals, and minimum for differential output signals.

Figure 4.20: Measured output current with different bias control voltage

Focusing at the output current in figure 4.20 for a supply voltage 0.8 V, we do notice the bias control does not affect the output current. This is because the inverter on the input is in strong inversion, however, as seeing in figure 4.21, it is possible to change the gain of the circuit.

This amplifier is implemented with the same building blocks as presented earlier, the inverter and the analog inverter, with $C_i = 18.4fF$, $C_r = 14.2fF$, $C_a = 18.4fF$ and $C_b = 10fF$
4.2. OTA WITH FLOATING-GATE CIRCUITS

4.2.4 Transconductance amplifier $V_{dd} = 0.8V$

The measured output voltage on $V_{out1}$ with different bias voltages and $V_{in2} = \frac{V_{dd}}{2}$, is shown in figure 4.22. The equilibrium current of the inverter Invl, is $0.4\mu A$. The output voltage swing is almost rail-to-rail, it is 12 mV from supply rail $V_{dd}$ and 8 mV from the rail $V_{ss}$. This gives a total voltage amplitude of 18 mV.

Figure 4.23, shows the effect of the bias control, as we can see it is possible to adjust the gain from $-0.6$ to $-2.7$. If we should need more amplification it is possible to make the floating gate capacitors on the input of the inverter $C_i$ and $C_a$ larger, or if we do need a larger dynamic adjustment range on the output, we could made the bias control capacitors $C_b$ larger.
Figure 4.22: Measured output voltage with different bias control voltage

Figure 4.23: Measured gain of the transconductance amplifier with dynamic load
4.2. OTA WITH FLOATING-GATE CIRCUITS

4.2.5 Transconductance amplifier $V_{dd} = 0.5V$

If we are reducing the power supply to $V_{dd} = 0.5V$ we do still have a proper output swing, as shown in figure 4.24. The equilibrium current on the inverter Inv1, is 120nA. The output signal is 14 mV from the rail $V_{dd}$ and 12 mV from the rail $V_{ss}$. This gives a total voltage output of 474mV.

![Figure 4.24: Measured output voltage with different bias control voltage](image)

The output gain with different bias voltage is shown in 4.25 when $V_b >> V_b^*$ the gain is $-0.70$ and when $V_b^* >> V_b$ the gain is $-2.1$. We do still have a reasonable dynamic range even with a 0.5 V supply voltage.
4.2.6 Transconductance amplifier $V_{dd} = 0.3V$

If we are using a supply voltage of only 0.3 V, we are approaching a limit of operation. The equilibrium current is 83 nA. The output signal is 17.5 mV from the rail $V_{dd}$ and 13 mV from the supply rail $V_{ss}$. The output voltage swing is still satisfying, and gives a total amplitude of 269.5 mV.

The measured gain in figure 4.27 is $-1.15$ to $-1.9$. We do notice that with reduced supply voltage, we get a reduced dynamic range of the bias control.
Figure 4.26: Measured output voltage with different bias control voltage

Figure 4.27: Measured gain of the transconductance amplifier with dynamic load
Frequency response of the Transconductance Amplifier

There is not done any measurements of the bandwidth of this circuit. The simulated frequency response with supply voltage $V_{dd}$ at 0.5 V, is presented in figure 4.28. The voltage gain is 8 dB, and the bandwidth is 1.5 MHz (+0/-3dB), with -60° phase shift as shown in figure 4.29. The Gain Bandwidth is 3.5 MHz and the phase shift is $-75^\circ$. This result indicates the stability of the circuit is satisfactory.

Figure 4.28: *Simulated frequency response of the transconductance amplifier with dynamic load*
4.3 Tanh Amplifiers

As mentioned in the introduction of this chapter, by making combinations of a \( \text{tanh} \) and a \( \text{sinh} \) OTA, it is possible to make a more linear amplifier. However, if we are going to use the same building blocks, we have to find a combination of the designed circuits which gives us a \( \text{tanh} \) shaped output current. The \( \text{tanh} \)-amplifier [13] gives us what we want. It is made by combining an analog inverter with a current sum circuit presented in chapter 3, and the output stage with the n-MOS and the p-MOS is just a summing circuit.

The Tanh amplifier is shown in figure 4.30 and figure 4.31. The simulated DC-characteristics is shown in figure 4.32. As we can see, it is possible to make a compact rail-to-rail FGUV MOS OTA, with \( \text{tanh} \) shaped current, which we can use as a single amplifier or combined with a sinh-amplifier to make a linear OTA.
Figure 4.30: The Tanh amplifier ver #1

Figure 4.31: The Tanh amplifier ver #2
4.3. TANH AMPLIFIERS

The output current of the tanh amplifier in figure 4.31 can be expressed:

\[ I_p = I_b \exp\left\{ \frac{k_b}{\kappa T} \left( \frac{V_{dd}}{2} - V_{dd} - V_1 \right) \right\} \times \exp\left\{ \frac{k_b}{\kappa T} \left( V_{dd} - V_x \right) \right\} \]

\[ = I_b \frac{\exp\left( \frac{k_b}{\kappa T} (V_1 - \frac{V_{dd}}{2}) \right)}{\exp\left( \frac{k_b}{\kappa T} (V_2 - \frac{V_{dd}}{2}) \right)} \]

\[ = I_b \frac{\exp\left( \frac{k_b}{\kappa T} (V_1 - \frac{V_{dd}}{2}) \right)}{\exp\left( \frac{k_b}{\kappa T} (V_1 - \frac{V_{dd}}{2}) + \exp\left( \frac{k_b}{\kappa T} (V_2 - \frac{V_{dd}}{2}) \right) \right)} \]

\[ I_n = I_b \frac{\exp\left( \frac{k_b}{\kappa T} (V_2 - \frac{V_{dd}}{2}) \right)}{\exp\left( \frac{k_b}{\kappa T} (V_1 - \frac{V_{dd}}{2}) + \exp\left( \frac{k_b}{\kappa T} (V_2 - \frac{V_{dd}}{2}) \right) \right)} \]

\[ I_{out} = I_p - I_n \]

\[ = I_b \frac{\exp\left( \frac{k_b}{\kappa T} (V_1 - \frac{V_{dd}}{2}) \right) - \exp\left( \frac{k_b}{\kappa T} (V_2 - \frac{V_{dd}}{2}) \right)}{\exp\left( \frac{k_b}{\kappa T} (V_1 - \frac{V_{dd}}{2}) + \exp\left( \frac{k_b}{\kappa T} (V_2 - \frac{V_{dd}}{2}) \right) \right)} \]

\[ = I_b \tanh\left\{ \frac{k_b}{\kappa T} (V_1 - V_{dd} - (V_2 - \frac{V_{dd}}{2})) \right\} \]

\[ = I_b \tanh\left\{ \frac{k_b}{\kappa T} (V_1 - V_2) \right\} \]

where \( k_o = k \) and \( I_b = I_{bec} \exp\left( \frac{k_b}{\kappa T} (V_b - \frac{V_{dd}}{2}) \right) \).

The simulated output current of the Tanh amplifier is shown in figure 4.33.
Figure 4.33: Simulated output current of the Tanh amplifier
Chapter 5

Conclusion and Further Improvements

5.1 Summary

This thesis has presented some fully functionals OTA’s, constructed with UV-Programmable Floating-Gate Transistors (FGUVMOS). The measured results are presented and analyzed.

5.1.1 FGUVMOS Design

The programming technique used to tune the FGUVMOS circuits is verified, and it is showed how easy it is to change the equilibrium current of different circuits.

The different building blocks like digital inverters, analog inverters and analog additive inverters constructed in FGUVMOS design, are working well on their own and do operate as expected. They have all rail-rail voltage swing, both on the input and on the output.

The DC-characteristics shows appropriate performance even with low-voltage operations. Theoretical these OTA’s may function with a supply voltage as low as 100mV ($4U_T$). The measured results with 0.3 V, which is far below any commercial OTA design, shows that the circuits are working as we could expect.

The AC-Characteristics is just simulated, but shows suitable results with a low-voltage supply. The designed OTA’s, have a bandwidth more than 2 MHz, and well controlled phase response, hence a stable constructed amplifier design.

We did face one problem in the UV-programming of the circuit; the different building blocks needed different programming voltages to operate together. Assuming an operation range with equilibrium current $I_{beo}$ in weak to moderate inversion, shown in the table with $V_{dd} = 0.5V$. 

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As focused in the table above, it is not easy to connect these blocks together, we do notice if we are building a block between a Digital inverter and an Analog additive inverter, it is not possible to make optimal combinations. One solution is to have separate supplys of different building blocks. This will make it possible to program the circuit, as we do expect.

### 5.2 Further Improvements

The objective of making a total linear amplifier, is possible by making OTA’s with the help of FGUVMOS transistors. We know by using combinations of a $\sinh$ and a $\tanh$ OTA’s, it is possible to increase the linearity, for instance by making the output current $I_{out}$ as a function $\sinh(\tanh(V_{in1} - V_{in2}))$, however, there is also another solution.

What if we could make an OTA with an $\text{arcsinh}$ shape, we could make an almost linear amplifier, hence $I_{out} = \sinh(\text{arcsinh}(V_{in1} - V_{in2}))$.

When we are going to program an analog or digital FGUVMOS circuit with UV-light, we want to use the supply rails as programming terminals, hence the same programming voltages on the entire chip. At this moment we have not solved this problem. Perhaps changing the length and width of the transistors, and changing the size of the UV-hole in different blocks, can be a solution. This is what we have to look more closely to in the future, and is left open for further investigation.

### The Future Plans

Working with this thesis, have made a growing interest for FGUVMOS design, which hopefully will lead to some interesting articles in the future.
Bibliography


