Delta-Sigma Modulators using Frequency-Modulated Intermediate Values

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Abstract—This paper describes a new first- and second-order delta-sigma modulator concept where the first integrator is extracted and implemented by a frequency modulator with the modulating signal as the input. The result is a simple delta-sigma modulator with no need for digital-to-analog converters, allowing straightforward multi-bit quantization. Without the frequency modulator, the circuit becomes a frequency-to-digital converter with delta-sigma noise shaping. An experimental first- and second-order modulator have been implemented in a 1.2-μm standard digital CMOS process and the results confirm the theory. For the first-order modulator an input signal amplitude of 150mV resulted in a SQNR of ≈115dB at 2MHz sampling frequency and signal bandwidth 500Hz.

I. INTRODUCTION

The delta-sigma (Δ-Σ) A/D conversion technique [?] is currently receiving increased attention as an attractive alternative to traditional A/D conversion. Although the delta-sigma modulator (DSM) is well suited for VLSI implementation, multi-bit quantization is not straightforward due to DAC linearity problems, and the sampling speed is limited by integrator and DAC slewing rates.

By implementing the main integrator as a frequency modulator [?, ?], we achieve a simpler circuit without DACs. Straightforward multi-bit quantization, and a potentially higher sampling frequency is one amongst other features. The new DSM that will be referred to as a frequency DSM (FDSM) becomes a F/D converter with Δ-Σ noise shaping if the frequency modulator is removed.

To illustrate why a frequency modulator can be used as an integrator we may look at the FM signal itself. An ideal FM signal may be expressed as

\[
fm(t) = \sin[\theta(t)],
\]

where

\[
\frac{\theta(t)}{2\pi} = \int_{-\infty}^{t} (f_c + kx(\tau))d\tau.
\]

In this expression \(f_c\) represents the carrier frequency, \(x(\tau)\) the modulating signal, and \(k\) the frequency sensitivity. From Eq. 2 we see that the FM signal variable \(\theta(t)/2\pi\) is the integral of \(f_c + kx(\tau)\).

For F/D conversion, the commonly used count-dump and reset converter is a useful device due to its simplicity and high speed potential. However, in a Nyquist-rate application the resolution-bandwidth product is low, and the signal is heavily low-pass filtered. The main theoretical result presented in this paper is that merely by raising the sampling frequency in the traditional count-dump and reset F/D converter, equivalent delta-sigma noise shaping will result with respect to the modulating signal. Compared to the ΔΣFDC reported in [?, ?] and the frequency discriminator in [?, ?], the first-order FDSM concept is simpler as both the ΔΣFDC and the frequency discriminator may be replaced by a counter, or as we will see by a D flip-flop, plus a subtractor.

By digitally correcting the first-order FDSM output bit or word stream by a phase controlled corrector, equivalent second-order delta-sigma noise shaping can be obtained. Compared to the second-order ΔΣFDC in [?, ?], the FDSM concept is still simpler as no N-bit ADC, amplifier, phase detector and S/H circuit are required. As opposed to the second-order architecture reported in [?, ?], the FDSM offers multi-bit quantization.

In Section II we describe the first-order FDSM concept by introducing three different DSMs using frequency modulated intermediate values. Section III describes the MASH-similar [?, ?] second-order solution. Both simulated and measured results are then presented in Section IV, and finally we present our conclusions in Section V.

II. THE FIRST-ORDER FDSM

In a traditional DSM the integrator is embedded in a high-gain feedback loop. In this way integrator saturation is avoided and circuit precision requirements are relaxed. In F/D applications where we want to replace the integrator with a frequency modulator, feedback over the frequency modulator will normally not be possible. However, a frequency modulator may be considered as a modulo-\(n\) integrator where there is no need for feedback to prevent saturation. And as we will see, even without feedback the FDSM concept will provide relaxed circuit requirements in some parts of the modulator.

To derive the non-feedback DSM version we may start by looking at the traditional first-order DSM. By considering the ideal behavior we may disregard the feedback DAC and represent the quantizer by the nonlinear quantizing function \(q()\) as illustrated in Fig. 1.

![Figure 1: An ideal first-order DSM model](image-url)
The output may now be expressed as
\[
y_n = q \left( \sum_{k=-\infty}^{n-1} (x_k - y_k) \right).
\] (3)

Since \(y_k\) is already quantized, it may be resolved from the quantizing function and represented as
\[
\sum_{k=-\infty}^{n} y_k = q \left( \sum_{k=-\infty}^{n-1} x_k \right),
\] (4)

which is equivalent to
\[
y_n = q \left( \sum_{k=-\infty}^{n-1} x_k \right) - q \left( \sum_{k=-\infty}^{n-2} x_k \right).
\] (5)

The corresponding non-feedback equivalent is illustrated in Fig. 2. This circuit illustrates the simple principle of the first-order DSM. After the unit delay, the modulator operates by first integrating the signal, then quantizing it, and finally differentiating the signal and the quantization error to restore the signal. Since the quantization error is not integrated it will be differentiated while the input signal passes unchanged.

In the non-feedback version there is no need for a DAC and thus no problems associated with inaccurate DAC output levels. As in Leslie & Singh’s single-bit feedback DSM [?], the output of the quantizer is digitally differentiated, and baseband noise introduced by misplaced quantizer thresholds will be heavily suppressed. These two features make the extension to multi-bit quantization straight-forward. By exchanging the integrator in Fig. 2 with the non-saturating frequency modulator, a practical

FDSM is formed as illustrated in Fig. 3.

In the FDSM the drawback is that due to the lack of feedback, all nonlinearities in the frequency modulator will add directly to the signal. In general, all frequency modulating noise will be un-shaped while phase modulating noise will be first-order shaped. In that sense the FDSM concept utilize the high noise immunity of FM systems.

If the FDSM is to be used as an alternative to a traditional analog-to-digital DSM, a very linear- and power-supply-noise-insensitive frequency modulator have to be used. However, for F/D applications, the integrator SNR will be given by the SNR of the FM signal and all excess noise will be first-order shaped.

A. \(\theta(t)/2\pi\) detection

To be able to use the frequency modulator as an integrator, a \(\theta(t)/2\pi\) detector must be applied. This quantity may be separated into
\[
\theta_n/2\pi = p_n + \phi_n,
\] (6)

where \(p_n\) is an integer representing the received number of rising FM edges at time \(n T_s\), and \(\phi_n \in [0, 1)\) is the phase difference between the previous rising FM edge and the sample signal edge scaled by \(1/2\pi\) (Fig. 4). The FDSM output may now be expressed as
\[
y_n = q \left( \frac{\theta_n}{2\pi} \right) - q \left( \frac{\theta_{n-1}}{2\pi} \right) = q(p_n + \phi_n) - q(p_{n-1} + \phi_{n-1}).
\] (7)

By choosing integer quantization thresholds, \(p_n\) and \(p_{n-1}\) will already be quantized and may be resolved from the quantizing function yielding
\[
y_n = p_n - p_{n-1} + q(\phi_n) - q(\phi_{n-1}).
\] (8)

But since \(\phi_n\) is restricted to the interval \([0, 1)\) and we are using integer quantization thresholds, the quantization error will be \(-\phi_n\) and the output from the quantizer function will always be zero, which let us reduce Eq. 8 to
\[
y_n = p_n - p_{n-1}.
\] (9)

This is simply the number of received rising FM edges or periods during the sampling interval.

From this we see that the most straight-forward FDSM implementation is a frequency modulator followed by a count and dump circuit. In other words, we have shown that merely by raising the sampling frequency in the traditional count and dump FDC system we obtain equivalent first-order delta-sigma noise shaping with respect to the modulating signal.

However, the frequency modulator is a continuous-time integrator, and the count and dump FDC system can therefore be shown to be mathematically equivalent to a conventional DSM with a continuous-time integrator and input \(T_s (f_c + k x(t))\). But for high oversampling ratios, we may approximate \(\theta_n/2\pi\) by \(T_s \sum_{i=-\infty}^{n} (f_c + k x_i)\), and the output will be
\[
y_n \approx q \left( T_s \sum_{i=-\infty}^{n} (f_c + k x_i) \right) - q \left( T_s \sum_{i=-\infty}^{n-1} (f_c + k x_i) \right).
\] (10)

By representing the quantization error by the additive noise source \(e_n\), the equation reduces to
\[
y_n \approx T_s (f_c + k x_n) + e_n - e_{n-1}.
\] (11)
As we see, the input signal \( x_n \) is just scaled and biased while the quantization error is differentiated.

The effective output word length will depend on the maximum output signal range, which can be expressed

\[
SR_o \approx 2\Delta f/f_s = k \cdot SR_i/f_s,
\]

where \( \Delta f \) is the maximum frequency deviation given by the maximum input signal range \( SR_i \). Together with the first-order shaped quantization noise \([3,7]\) the signal to quantization noise ratio will be

\[
SQNR \approx 20 \log \left( \frac{SR_o}{2\sqrt{2}} \right) - 20 \log \left( \frac{\pi}{6} \left( \frac{f_{\text{max}}}{f_s} \right)^{3/2} \right).
\]

where \( f_{\text{max}} \) is the maximum frequency of the modulating signal \( x(t) \). From Eq. 12 we see that by doubling \( f_s \) we only increase the \( SQNR \) by \( \approx 3 \text{dB} \) due to the reduced \( SR_o \). A more efficient way to increase the \( SQNR \) is to increase the integrator gain by the frequency sensitivity \( k \). By increasing the carrier frequency \( f_c \), a high \( k \) combined with a low maximum relative frequency deviation will result, which normally will improve the linearity of the frequency modulator for a fixed output range.

### B. The Basic Modulo FDSM

With modulo-\( 2^n \) counting (Fig. 5), \([3,7]\), we omit the speed limiting reset operation, and the output signal bias component due to \( f_c \) will be clipped down to mod-\( 2^n \left( f_c/f_s \right) \). By using modulo arithmetic, the only restriction on the module \( 2^n \) of the counter is that it must be larger or equal to the difference between the maximum and minimum number of counts during the sampling interval. If not, there will be aliasing. We may therefore let the counter pass through several cycles during the sampling interval as long as the maximum frequency deviation is small enough to be accommodated by the module of the counter.

### C. The D Flip-Flop FDSM Variant

A simple way to double the resolution is by counting both rising and falling FM edges. For systems where the sampling frequency is more than twice the maximum FM frequency, the counter outcome will be restricted to zero and one, and a modulo-2 or one-bit counter will be sufficient. A one-bit counter counting on each signal edges may be implemented by a D flip-flop, and a one-bit subtractor without carry by a XOR gate. The entire FDSM may then be implemented as illustrated in Fig. 6.

The output will be HIGH when a FM edge is received and LOW otherwise. By rising the sampling frequency, the output will therefore approach a digitized representation of the FM

\[
Y_n = P_n - P_{n-1}
\]

\( n \)-bit (no borrow)

**Figure 5: The basic modulo-\( 2^n \) FDSM**

\( x(t) \)

\( \text{freq} \)

\( \text{mod} \)

\( \text{mod-}2^n \text{counter} \)

\( \text{n-bit} \)

\( \text{reg} \)

**Figure 6: The D flip-flop FDSM**

**Figure 7: D flip-flop intermediate/output signals. Top: modest \( f_s/f_c \) ratio, bellow: high \( f_s/f_c \) ratio.**

System level simulations indicate that constant FM duty cycle diversions from 50/50 is not noticeable in the output noise spectrum. However, as the duty cycle approaches 100/0 or 0/100, the signal power will be reduced by \( \approx 6 \text{dB} \).

### D. The Pointer-FDSM Variant

In some applications, the FM signal can be generated by a ring oscillator where the delay of each inverter is modulated by the input signal. Examples are FL-ring oscillators \([3,7]\), and ring oscillators where the carrier mobilities in inverters located on a membrane is directly modulated by stress due to some physical parameter (acceleration, pressure, ..). By using the inverter power supply voltage as the input signal, the frequency of an ordinary CMOS inverter-based ring oscillator may also be approximated by a linear function of the input voltage in a limited range.

Considering the ring oscillator itself as an modulo-\( n \) counter, we both simplify the architecture and increase the resolution. This can be achieved by sampling the node values with D flip-flops and generating the logical XNOR between each neighboring node giving an active high “pointer” output that will run through all nodes in sequence (Fig. 8). The output may then be fed to a simple binary encoder followed by a differentiator. Since we cannot use modulo-\( 2^n \) counting, a modified subtractor must be used as indicated in Fig. 9.

**Figure 8: The different states of a 3-inverter ring oscillator**
For the Pointer-FDSM the $SR_o$ will be approximately

$$SR_o \approx \frac{2\Delta\tau}{f_s\tau_0},$$

(14)

where $\tau_0$ is the un-modulated delay of one inverter, and $\Delta\tau$ is the maximum relative delay diversion of one inverter. Simulations show insignificant $SNR$ reduction for minor relative constant diversions between the $\tau_0$ values.

In all FDSM variants, sampling clock phase noise (clock jitter) will be first-order noise shaped, while sampling clock frequency noise will be un-shaped. The sampling clock must therefore be considered as an frequency reference unless a reference modulator is used.

### III. The Second-Order FDSM

Using the same principles which gave rise to the first-order FDSM, an alternative second-order DSM may be designed. Fig. 10 illustrates a circuit that, except from a scaling factor, is a mathematical equivalent to a second-order MASH DSM, with integer quantization thresholds. The first-stage is implemented as a first-order FDSM, and the input to the second-stage is the negative quantization error $\phi_n$. The output can now be expressed as

$$y_n = p_n - p_{n-1} + \phi_n - \phi_{n-1} + \epsilon_n - 2\epsilon_{n-1} + \epsilon_{n-2},$$

(15)

where $\epsilon_n \in [0, 1]$ is the second-stage quantization error. As in the first-order case, $p_n - p_{n-1}$ may be approximated by Eq. 11, and the output may then be written as

$$y_n \approx T_n(f_c + k_{x_n}) + \epsilon_n - 2\epsilon_{n-1} + \epsilon_{n-2}.$$  

(16)

By considering the modulating signal $x_n$ as the input, we have a second-order DSM where the input is scaled and biased, and the quantization error $\epsilon_n$ is differential to the modulation signal.

The $SR_o$ will be given by Eq. 12, and the $SQNR$ will from [?] be

$$SQNR \approx 20 \log \left( \frac{SR_o}{2\sqrt{2}} \right) - 20 \log \left( \frac{\pi^2}{\sqrt{60}} \left( \frac{2f_{\text{max}}}{f_s} \right)^{5/2} \right).$$

(17)

By doubling $f_s$, we notice that we only gain $\approx 9$dB due to the reduced $SR_o$.

If the signal source itself contains a frequency modulator, we have shown that for F/D conversion or digital FM demodulation, we achieve equivalent second-order $\Delta-$Sigma noise shaping with respect to the modulating signal by using an oversampled count, dump, and reset F/D converter with a phase controlled corrector.

### A. The Second-Stage Implementation

The phase-input ($\phi_n$) to the second-stage modulator is not a directly measurable quantity, and therefore, probably the simplest way to compute $\phi_n$ is by the estimation

$$\phi_n \approx \Delta t_n / T_n^m.$$  

(18)

where $\Delta t_n$ is the time difference between the previous rising FM edge and the current sampling edge, and $T_n^m$ is the current FM period. It is hard to detect if the current rising FM edge is the last one before the sampling edge, and it is therefore easier to use the complementary phase $1 - \phi_n$, estimated by the time difference between the next rising FM edge and the sampling edge divided by $T_n^m$. By doing so, the second-stage output must be subtracted from the first-stage output.

Since the internal values in the accumulator are derived from time differences, the most convenient implementation is capacitor charging by a reference current during the measuring time interval. In this way accumulation and subtraction is, in principle, straight-forward. The problem is, however, properly scaling of the reference current. The reference current must be scaled to make the resulting capacitor voltage match the quantization thresholds. Due to signal dependent variations in $T^m$, the reference current should also be temporally adjusted according to these variations.

A much simpler approach is to use a constant reference current $I_{\text{ref}}$, and use the same $I_{\text{ref}}$ to implement the feedback by discharging the capacitor during some nearby $T^m$ interval, assuming that $T^m$ is approximately the same for adjacent FM periods (Fig. 11). By doing so, a scaled feedback representing -1 is carried out, and by doing nothing a feedback of 0 is carried out corresponding to the equivalent DAC levels 1 and 0. In this way the feedback signal is scaled to always match the input, giving an approximately correct bit-stream output regardless of the magnitude of the reference current assuming $f_c \gg f_{\text{max}}$.

By using only one charging current, and one voltage reference, there will be no linearity or matching restrictions on the capacitor. Noise introduced in the accumulator and counter, including thermal noise and sampling clock phase noise, will be first-order noise shaped. Sampling clock frequency noise will have the same impact on the signal as in the first-order FDSM.
The digital control logic in Fig. 12 enables $f_s$ or $f_m(t)$ access to the current switch.

To avoid inaccurate capacitor charging due to sloppy edges, we may use overlap charging illustrated by $Q_b+$ and $Q_b-$ in Fig. 13. These intervals, determined by the positive FM period, may also avoid metastability problems. Given an accurate current mirror, errors introduced by asymmetric sloppy edges will contribute with a constant charge bias. This offset will be equal for all samples, and should be almost eliminated by the differentiator.

**IV. Measured and Simulated Results**

**A. First- and Second-Order FDSM Simulations**

To verify the theory and simulate the ideal behavior, all FDSM variants have been simulated in the mathematical analysis tool Matlab[J]. The frequency modulator has been modeled as ideal, and practical effects such as nonlinearity are therefore not present. The power spectral density (PSD) has been estimated from $2^{18}$ samples of the simulated output bit/word streams multiplied by a six term Blackman-Harris-Hodie window. All plots are then normalized to let 0dB correspond to maximum signal amplitude.

In Fig. 14, the output PSD is shown for a basic modulo-4 FDSM where the input is a single sinusoidal signal with maximum amplitude and frequency 1.7KHz. The maximum input amplitude is defined to produce a relative frequency deviation of 10%. As we see, the noise spectrum is shaped according to first-order delta-sigma theory.

In Fig. 15 the output PSD is shown for a D flip-flop FDSM with a maximum relative frequency deviation of 10%. Again we notice the delta-sigma behavior. The high frequency excess noise is supposed to be a function of the output dynamic range location (0.72-0.88) relative to the quantization levels at 0 and 1.

By modeling the node signals of the Pointer-FDSM as phase-shifted FM square waves, a 15-inverter Pointer-FDSM has been simulated. A 3.33ns inverter propagation delay was chosen which corresponds to an overall carrier frequency of 10MHz. The resulting PSD is shown in Fig. 16.
For the second-order FDSM PSD shown in Fig. 17 we recognize the 40dB/decade slope of the noise spectrum which is characteristic for the second-order DSM.

B. First- and Second-Order FDSM Measurements

A 15-inverter Pointer-FDSM front-end (ring oscillator, D flip-flops, XNOR and binary encoder) has been implemented in a standard 1.2-μm digital CMOS process. The main objective with this implementation has been to verify the principle, and the most straight-forward architecture where the ring oscillator frequency is modulated by the inverter power supply voltages was chosen. In Fig. 18 one of 15 sections corresponding to the left part of Fig. 9 is shown. The modulo-15 differentiator is implemented in software.

To reduce transistor flicker-noise in the ring oscillator, the p- and n-transistor area in each inverter where chosen as large as [math]3\mu m \times 222\mu m[/math] and [math]11.2\mu m \times 298\mu m[/math] respectively. With these dimensions, the carrier frequency was found to be [math]\approx 10MHz[/math]. A reference FDSM running at a constant frequency was included to reduce common-mode noise.

With a sampling frequency of [math]2MHz[/math] and a [math]\Delta f/f_c[/math] ratio of 10%, the input dynamic range was found to be [math]\approx 300mV[/math] and the range [math]4.7-5V[/math] was then chosen. For this input range, the maximum relative nonlinearity of the ring oscillator was, by a DC scan, measured to [math]\approx 0.2%[/math].

In Fig. 19 the measured output PSD is shown for a single sinusoidal input signal at 72Hz. The first plot illustrates the output PSD for an input signal amplitude as low as [math]\approx 0.25V[/math]. From the plot we conclude that for these transistor dimensions, the effect of ring oscillator transistor noise is insignificant compared to the quantization noise for frequencies above 7Hz. By increasing the signal amplitude up to 150mV, the nonlinear power supply voltage/frequency relationship of the ring oscillator appear clearly as shown in Fig. 20. Table 1 presents test-chip specifications for two different input signal ranges.

The F/D sub-circuit of a second-order FDSM have also been implemented in a standard 1.2-μm digital CMOS process. A charging/discharging scheme corresponding to Fig. 13 was applied. In Fig. 21, the content of the control logic from Fig. 12 is shown. A /S/R flip-flop is used to decide if the positive edge of the sampling clock has arrived at the start or at the end of a FM period. To generate the necessary control signals, a double-edge clocked P/N-C2MOS shift register [?] is applied. The comparator architecture is shown in Fig. 22.

So far the circuit has only been tested for DC or constant frequency inputs by the use of a crystal oscillator. However, by looking at the plot in Fig. 23, we notice that the complete quantization noise spectrum is maintained, which indicates the presence of a sufficient amount of dithering noise to randomize the
input to the accumulator. If the phase input is sufficiently randomized, the accumulator will not “see” any difference between a modulated input signal and the constant frequency from the crystal oscillator. Since no increase in noise is expected from the first stage by applying a modulated input, the idle channel measurements are therefore assumed to provide valuable information of the performance even for modulated inputs.

With a chosen second-stage current/capacitor ratio of $4\mu\text{A}/1\text{pF}$, the FDSM was found to accommodate an input frequency range of 3-20MHz. A simple cascode current source together with minimum-transistor current switches was used. The total power dissipation was measured to $\approx 320\mu\text{W}$.

Again, to reduce common-mode noise, a reference FDSM was included. Unfortunately, due to pad limitations, the maximum sampling frequency for both the first- and second-order test circuits have been limited to 2MHz.

By comparing the measured noise spectrum to the ideal simulated spectrum, they are almost identical for frequencies above 1KHz. For frequencies below 1KHz, a noise floor at $\approx 160$dB appears. This excess noise is supposed to be the result of inaccurate analog components in the second-stage.

In Fig. 24 a photomicrograph of the test-chip containing the Pointer-FDSM front-end and the second-order FDSM F/D-subcircuit is included.

V. Conclusion

By extracting the first integrator and using frequency as an intermediate value, a new DSM architectural concept is presented. The resulting architecture may be used both for analog-to-digital and frequency-to-digital conversion.

A. Delta-Sigma Analog to Digital conversion

Compared to the first-order traditional DSM, the first-order FDSM has the following advantages:

- Multi-bit quantization with no DAC, very simple implementation in standard digital CMOS, very high sampling frequency potential, suited for low power supply voltage operation, potential of low power consumption.

The high sampling frequency potential may be utilized either to achieve a higher SQNR for a given signal bandwidth, or to increase the signal bandwidth for a given SQNR.

Compared to the second-order MASH DSM the second-order FDSM has the following advantages:

- Extended multi-bit quantization with no DACs, no stage matching problems, simpler implementation in standard digital CMOS, only one capacitor needed with very low precision requirements, higher sampling frequency potential.

Used as an analog-to-digital converter, the main disadvantage of the FDSM concept is:

- Nonlinearities in the frequency-modulator/VCO adds directly to the signal.

Concerning linearity, we have conveyed the challenge of making a linear multi-bit DAC over to making a linear frequency-modulator/VCO. However, in a FDSM, the relative linearity of the frequency-modulator/VCO may be significantly improved by reducing the maximum relative frequency deviation ($\Delta f/f_c$). The resulting decrease in SQNR may be compensated by increasing the sampling frequency. If a ring oscillator-based frequency-modulator/VCO is used, we also hope that by increasing the carrier frequency, keeping the same maximum frequency deviation, the relative linearity will increase due to the decreased ($\Delta f/f_c$).

We have shown an example where the poor absolute linearity of a power-supply modulated CMOS-inverter ring oscillator provided an overall THD of about -80dB. In this example, the
sampling-frequency/carrier-frequency was just 2MHz/10MHz respectively.

**B. Direct Delta-Sigma Frequency-to-Digital Conversion**

For F/D conversion or digital FM demodulation we have shown that first-order $\Delta-S$ noise shaping will result merely by introducing oversampling in the traditional count and dump F/D converter. Second-order $\Delta-S$ noise shaping may also be achieved by adding a second-stage acting as a phase controlled corrector.

**Acknowledgment**

Thanks to Trond Sæther and the guys at Nordic VLSI for their interest and technical discussions, and thanks to Schlumberger Geco-Pracla for financing the ASIC work. We also want to gratefully acknowledge the reviewers for their very constructive comments.

**References**


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His main interest is micropower analog VLSI design. The main focus is large scale integration of analog (signal) processing in standard CMOS technology. Special features like weak inversion (subthreshold) operation permanent analog storage implemented with floating-gate techniques is explored. Both biology-inspired and artificial neural networks with adaptation is explored as paradigms for analog systems.

Tor Sverre is a member of IEEE and has served in several technical program committees as well as reviewer for several journals.

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Figure 19: Measured spectrum for Pointer-FDSM. Top: Input amplitude \( \approx 0.25 \mu V \), center: 2.7mV, bottom: 150mV. \( f_i = 2 MHz \), \( f_c \approx 10 MHz \).
Figure 20: Measured SQNR versus input amplitude for Pointer-FDSM. BW=500Hz

Figure 22: Comparator for second-order FDSM

Figure 23: Measured spectrum for second-order FDSM. $f_s = 2MHz$, $f_c = 19.66MHz$

Figure 24: First- and second-order FDSM test-chip die-photo. Right half: Reference circuits

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<th>TABLE I</th>
<th>POINT-FDSM TEST-CHIP SPECIFICATIONS</th>
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<tbody>
<tr>
<td></td>
<td>Max. input signal amplitude 2.7mV</td>
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<td>Signal bandwidth</td>
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<td>SQNR</td>
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<td>Die area</td>
<td>2.0x2.4mm$^2$</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>5V</td>
</tr>
<tr>
<td>Technology</td>
<td>1.2µm CMOS single poly</td>
</tr>
</tbody>
</table>